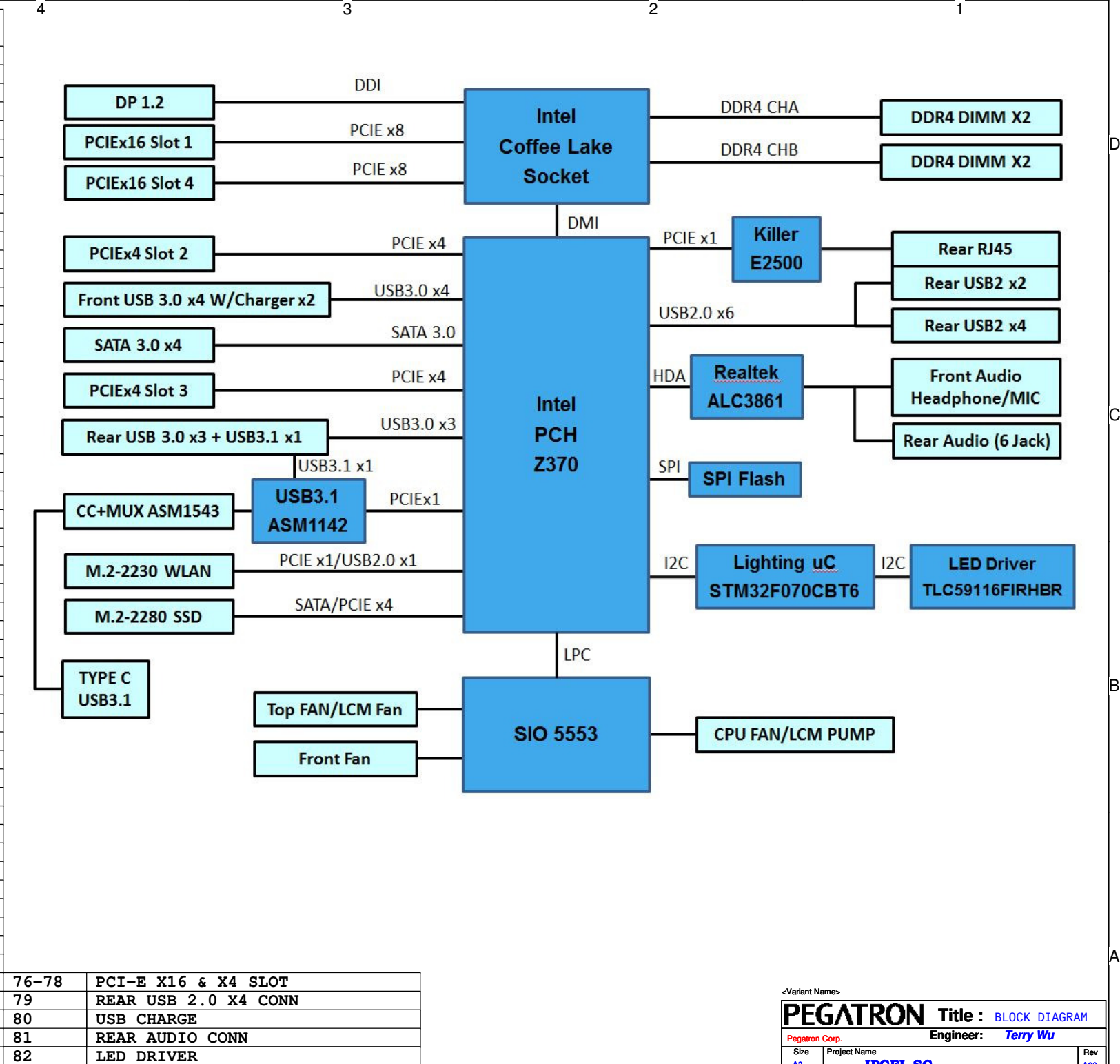


IPCF⁵L-SC

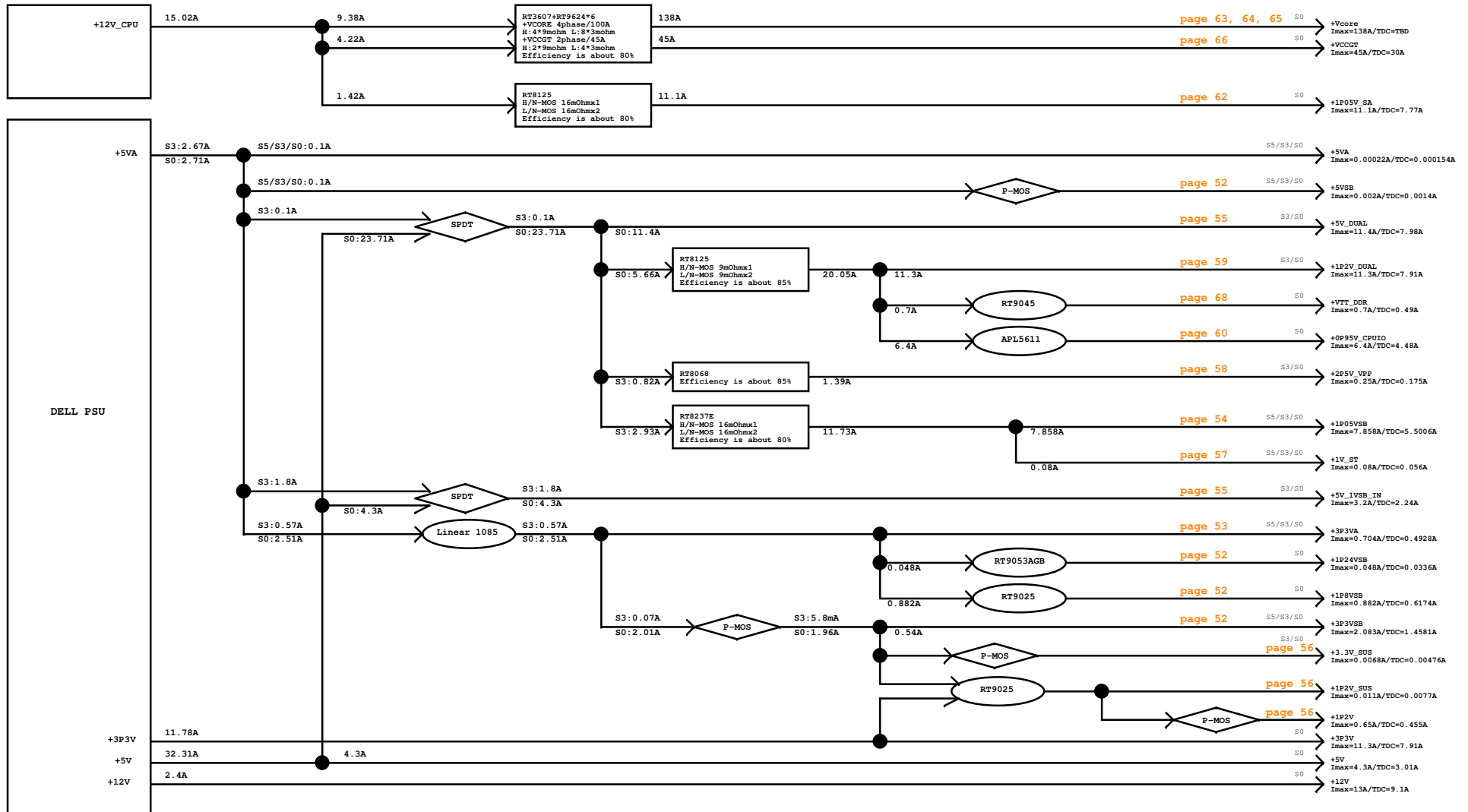
Revision: A00

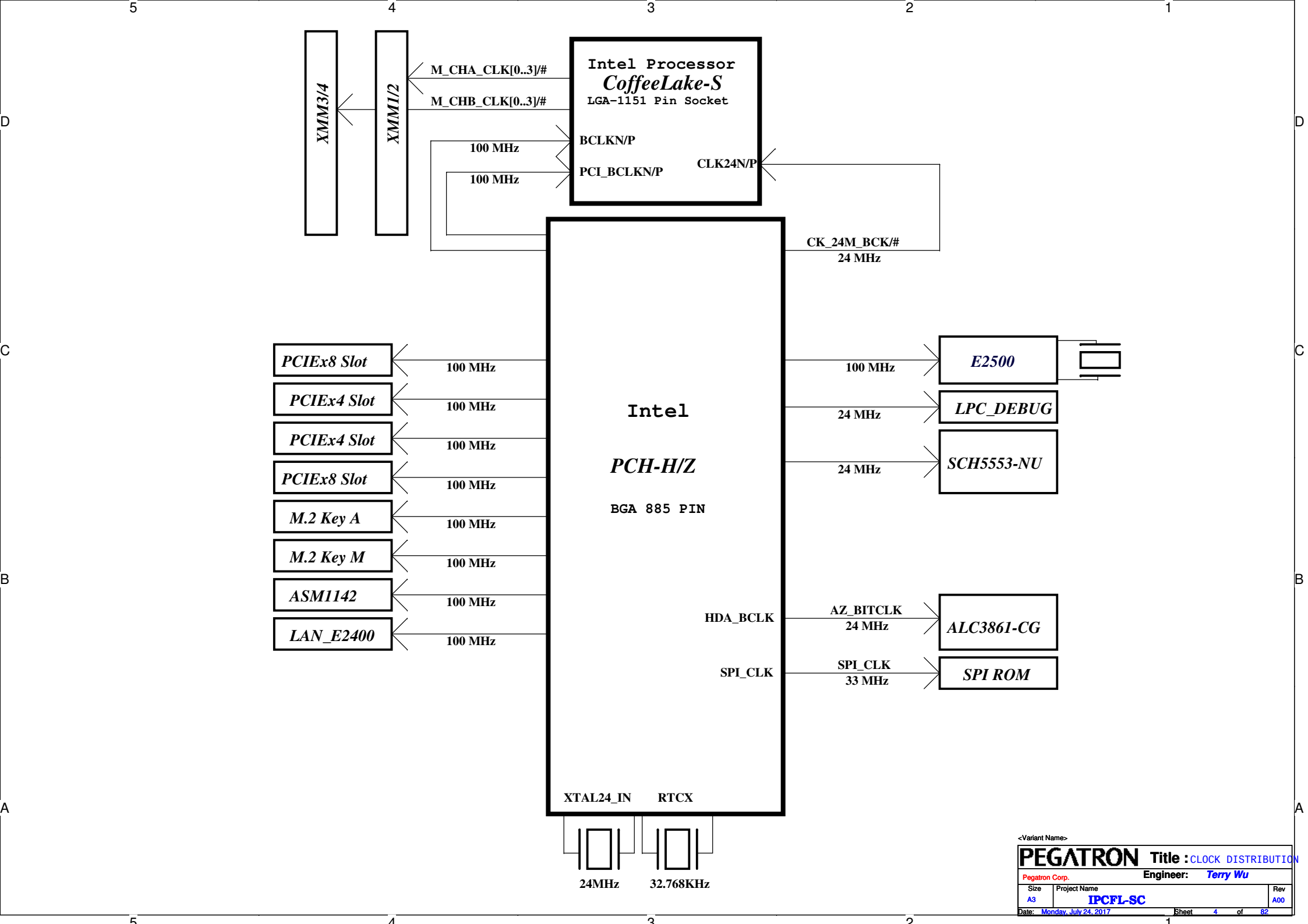
PAGE	TITLE
01	BLOCK DIAGRAM
02	CHANGE HISTORY
03	POWER FLOW
04	CLOCK DISTRIBUTION
05	POWER SEQUENCE
06	POWER DISTRIBUTION
07~12	CPU
13~17	DDR4
18~25	PCH
26	ME_Disable
27	RTC/CMOS/INTRUDER
28	SPI ROM
29	XDP
30	PWRBTN/RSTBTN
31	M.2 KEY A WLAN
32	M.2 KEY M SSD
33	PCI-E X16 SLOT1
34	AUDIO CODEC ALC3861-CG
35	FRONT AUDIO HEADER
36	ASM1142
37	ASM1543
38	XXXX
39	REAR TYPE C CONN
40	LAN_E2500
41	RJ45+USB2.0X2 CONN
42	REAR USB3.0X4 CONN
43	FRONT USB3.0 x 2 CONN -1
44	FRONT USB3.0 x 2 CONN -2
45	SATA CONN x 4
46	DP DONGLE CONTROL
47	DISPLAY PORT
48	SIO SCH5553-UH
49	LPC DEBUG HEADER
50	HDD/SSD LED
51	LED FOR DEBUG
52-53	+5VSB/+3VSB/+3VA
54	+1VSB
55	+5V_1VSB_IN & +5V_DUAL
56	+1P2V/+1P2V_SUS/+3.3V_SUS
57	+1V_ST
58	VCORE & VGT
59	+1P2V_DUAL
60	+0P95V_CPUIO
61	ATX POWER 24P CONN
62	+1P05V_SA
63-67	VCORE & VGT
68	VTT_DDR
69	MAIN POWER DISCHARGE
70	XXXX
71	FAN CIRCUIT/LIQUID PUMP
72	XXXX
73	SCREW HOLE
74	GFX PWR
75	Lighting Micro-Controller



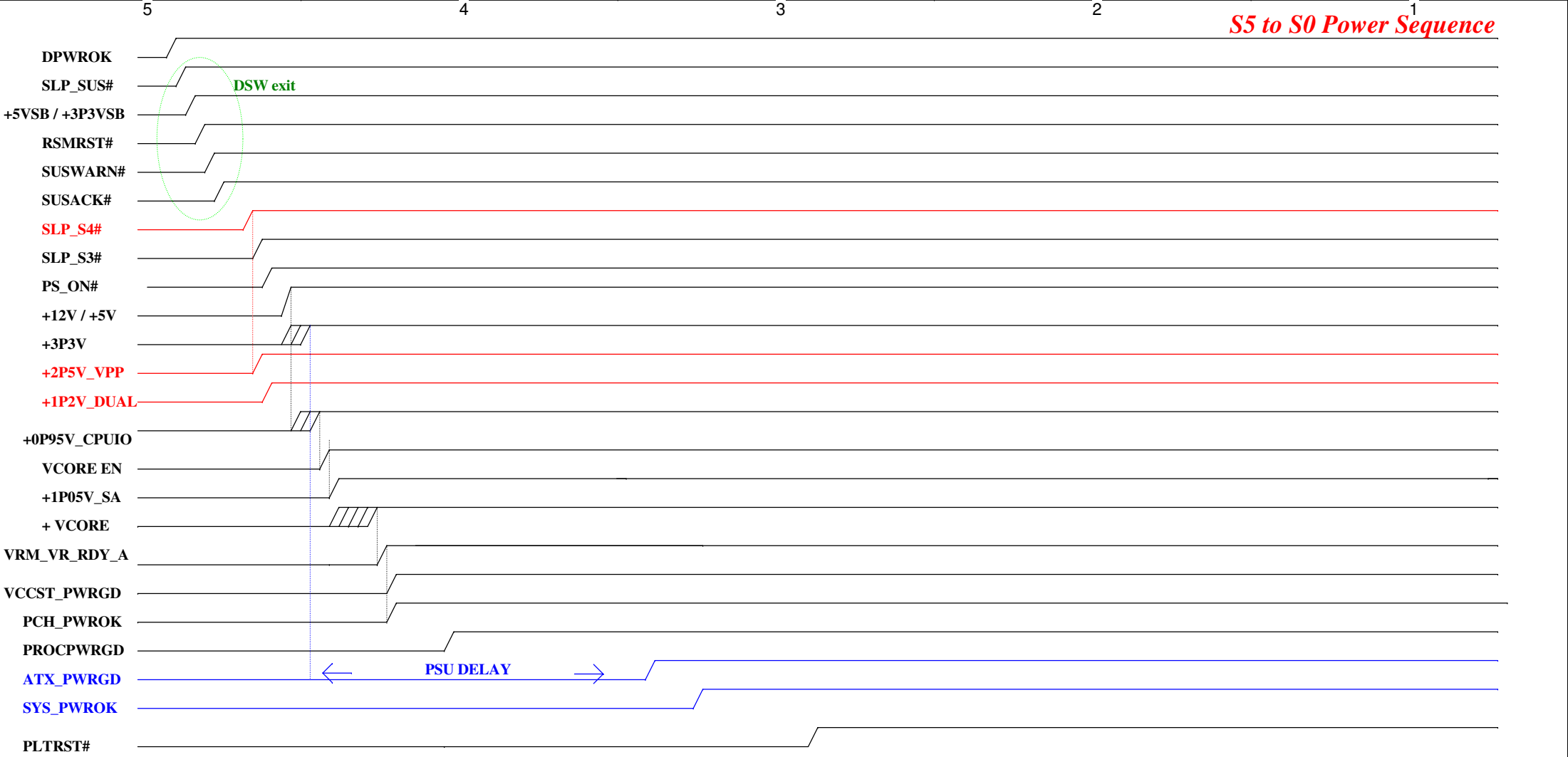
Schematics ⁵Change History

Version	Date	Page	Comments
X00	2017/05/17	75	Add uC Lighting micro-controller
X00	2017/05/17	7-12	Change CPU form KBL to CFL
X00	2017/05/17	39,42,43,44	Add AC caps for USB3.0/3.1 RX
X00	2017/05/17	39,42,43,44	Add common mode choke for USB3.0/3.1 TX form RF request
X00	2017/05/17	40	Change LoM from E2400 to E2500
X00	2017/05/17	48,73,75	Add Chassis Intrusion function
X00	2017/05/17	71	Add U.2 Blower
X00	2017/05/17	43, 44	Change front IO Power Cap from 2.2uF x2 to 100uF
X00	2017/05/17	43	Change USB3.0 header (P24) pin define for optimizing cable routing
X00	2017/06/26	39	Change Type-C CMC from 90 ohm to 67 ohm
A00	2017/07/20	31, 32, 42	Follow DFM rule, AC39, M2C14, M2C17, M2C2, M2C20, M2C5, O2CB10, O2CB11, O2CB16, O2CB2, O2CB7, O2CB8, UCB23 are changed from 0201 to 0402.
A00	2017/07/20	19	Update Board ID, install SR7698, SR712 and remove R545, SR7696.
A00	2017/07/20	77	Install SR7682, SR7683 for TBT3 card.
A00	2017/07/20	42, 43, 44	UC981, UC982, UC983, UC984, UC985, UC986, UC987, UC988, UC993, UC994, UC995, UC996 are changed to 330nF/10V for DELL recommend.
A00	2017/07/20	39, 43	UC975, UC976, UC977, UC978, UC979, UC980 are changed to 0 ohm for DELL recommend
A00	2017/07/20	71	Change pin define for blower device (KSB05105HC76J)
A00	2017/07/20	75	Follow ARD define to remove this feature
A00	2017/07/20	80	UR69742, UR69741, UR69744, UR69746, MQ34, MQ36, UR69743, UR69745 are removed to fix BITs BITS336329
A00	2017/07/20	20, 48	Follow EMC team requirement, SC141, SC147: 20pF/50V; SCB68: 47pF/50V
A00	2017/07/20	35	Follow codec vendor requirement, AR5, AR6 are changed from 1K ohn to 75 hm.
A00	2017/07/24	10, 20, 23, 28, 33, 40, 41, 76, 77, 78, 79	XR15, CR17, F3R14, F3R20, F3R21, F3R7, F3R8, HR17, HR18, LR20, LR22, M2R40, SR4, SR44, SR747, SR80, SR81, SR82, SR85, M2R41, XR11, M2R43, M2R44 are changed from 0 ohm to short pin.





S5 to S0 Power Sequence



	CPU CaffeLake-S 65W/95W
+VCORE	-> 138A (I _{max})
+0P95V_CPUIO	-> 6.4A (I _{max})
+1P05V_SA	-> 11.1A (I _{max})
+V_AXG	-> 45A (I _{max})

	PCH Z370
+1VSB	-> 7.858A
+3P3V	-> 0.007A
+3P3VSB	-> 0.78A
+3P3VA	-> 0.20A
+BATT	RTC(G3) -> 6uA

	DDR4-2667(4) & Termination
+1P2V_DUAL	-> 8A
+VPP(2.5V)	-> 0.25A
+VTT_DDR(0.75V)	-> 0.7A

	PCI Express x 16 (75W)
+12V	-> 5.5A
+3P3V	-> 3.0A
+3P3VSB	WAKE -> 0.375A No WAKE-> 20mA

	PCI Express x 4 (25W)
+12V	-> 2.0A
+3P3V	-> 1.0A
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	PCI Express x 4 (25W)
+12V	-> 2.0A
+3P3V	-> 1.0A
+3P3VSB	WAKE -> 0.375A - 1.24W No WAKE-> 20mA - 66mW

	PCI Express x 16 (75W)
+12V	-> 5.5A
+3P3V	-> 3.0A
+3P3VSB	WAKE -> 0.375A No WAKE-> 20mA

+5V_DUAL	REAR USB2.0 6 PORTS
	->3A

+5V_DUAL	REAR USB3.0 4 PORTS
	->3.6A

+3P3V	M.2 SSD / M.2 WIFI
	-> 0.9A / 0.6A

+3P3VSB	Killer E2500
	-> 0.151A

+5V_DUAL	REAR TYPE C
	->3A

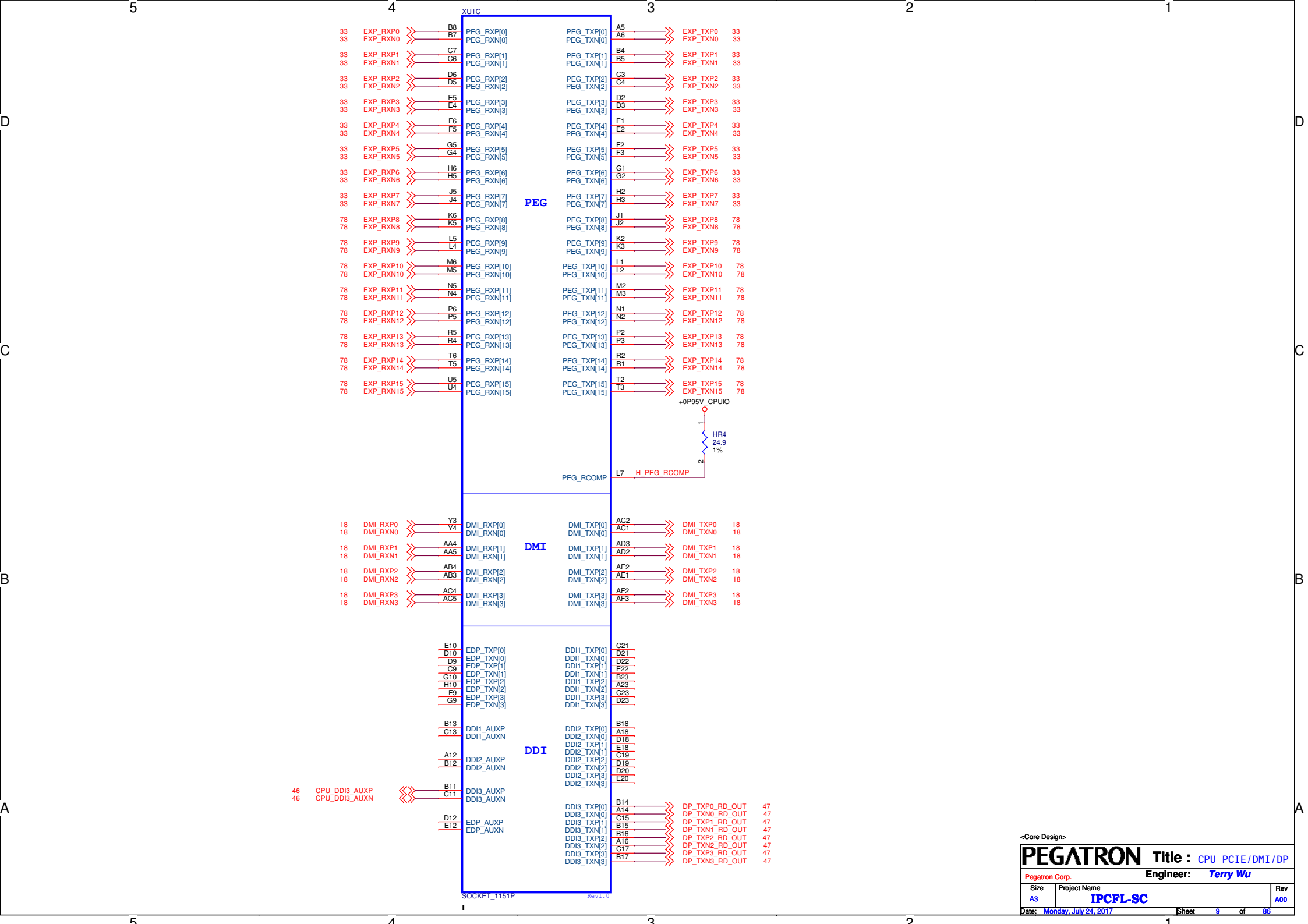
+12V_CPU	TOP FAN
	-> 0.8A

+12V_CPU	PUMP/CPU FAN
	-> 0.208A / 0.7A

+12V_CPU	GFX FAN
	-> 0.8A

+5V_DUAL	FRONT USB3.0 2 PORTS
	->1.8A

+5V_1VSB_IN	FRONT USB3.0 2 PORTS Charge
	->3.2A



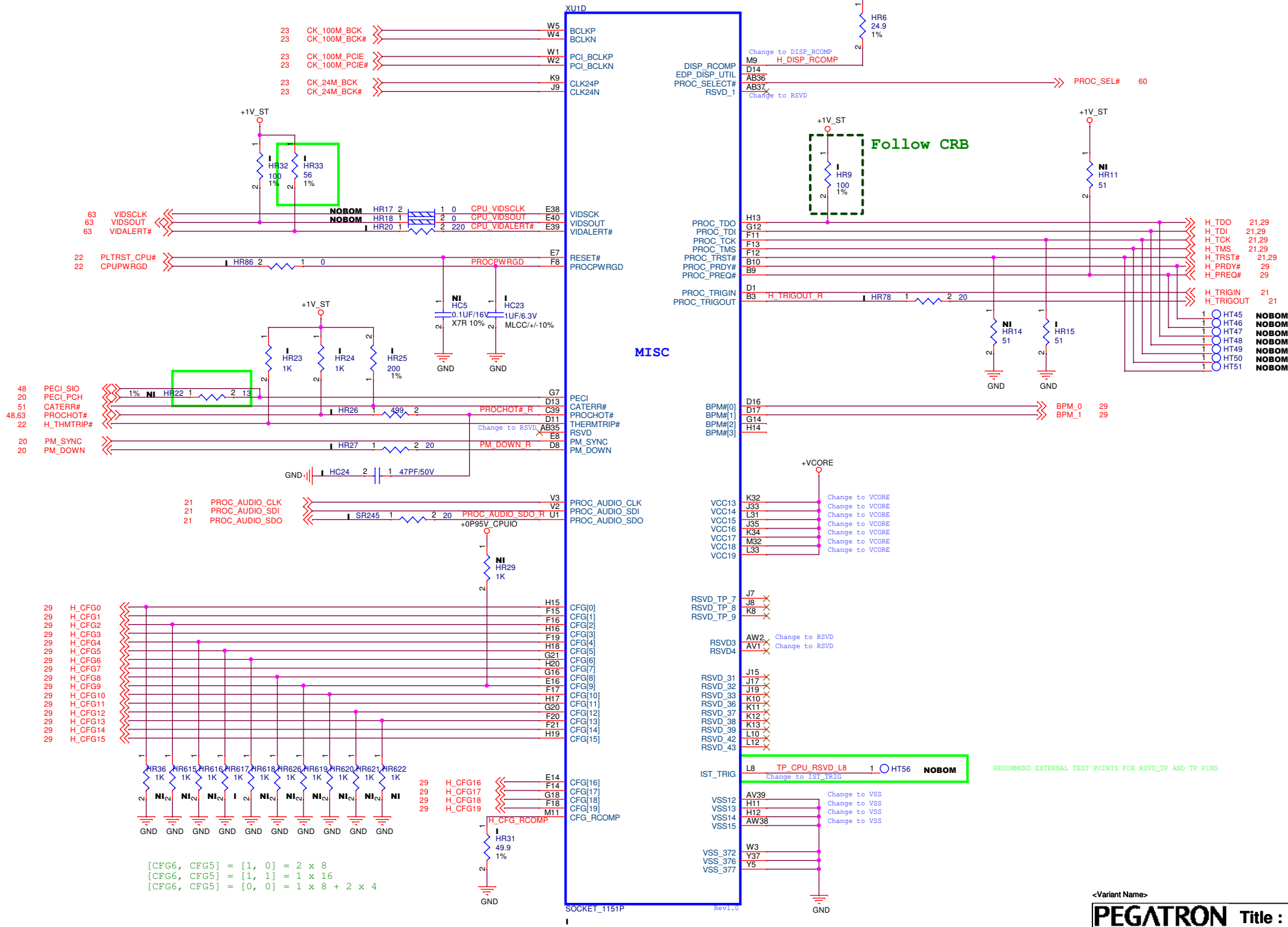
<Core Design>

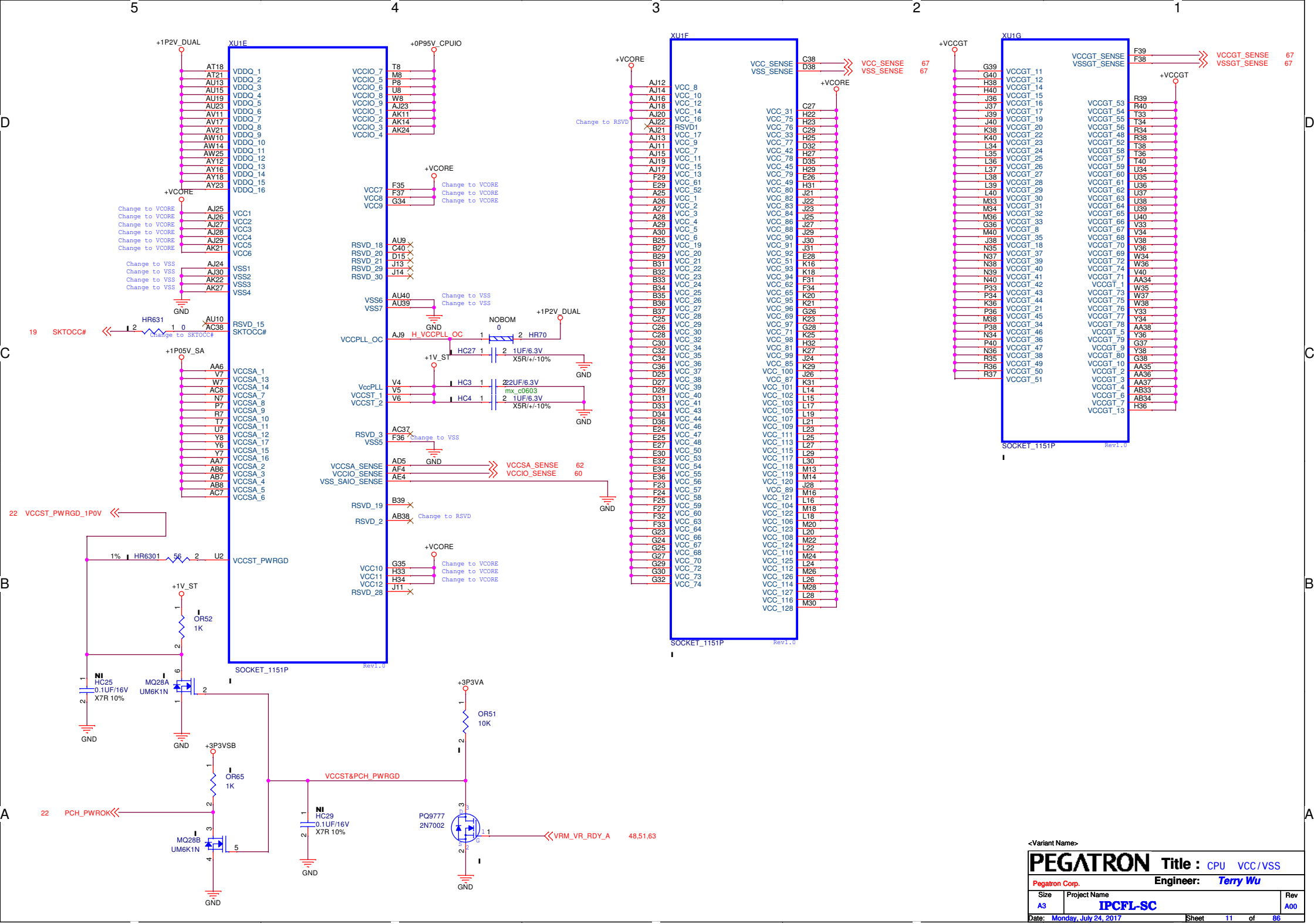
PEGATRON Title : CPU PCIE/DMI/DP

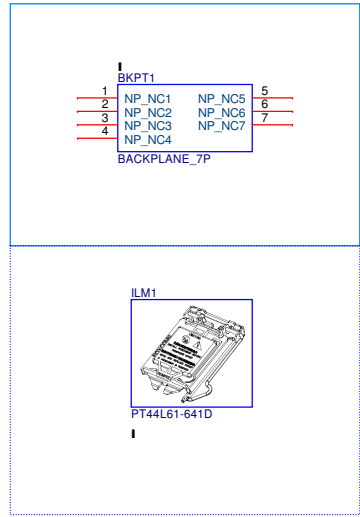
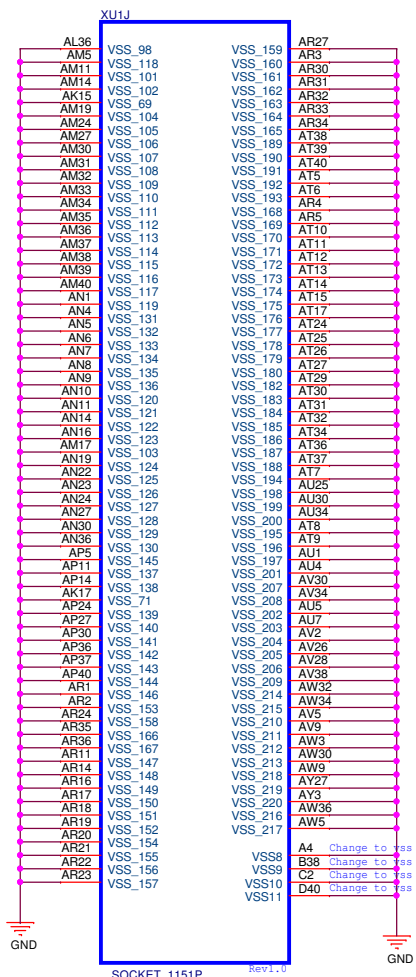
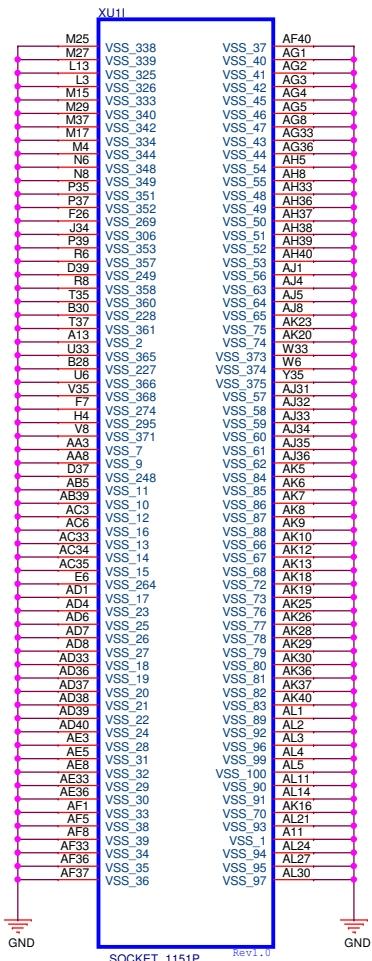
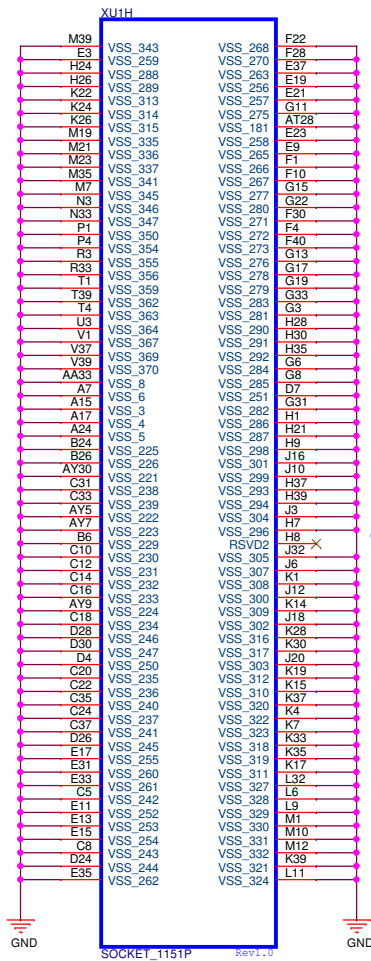
Pegatron Corp. Engineer: Terry Wu

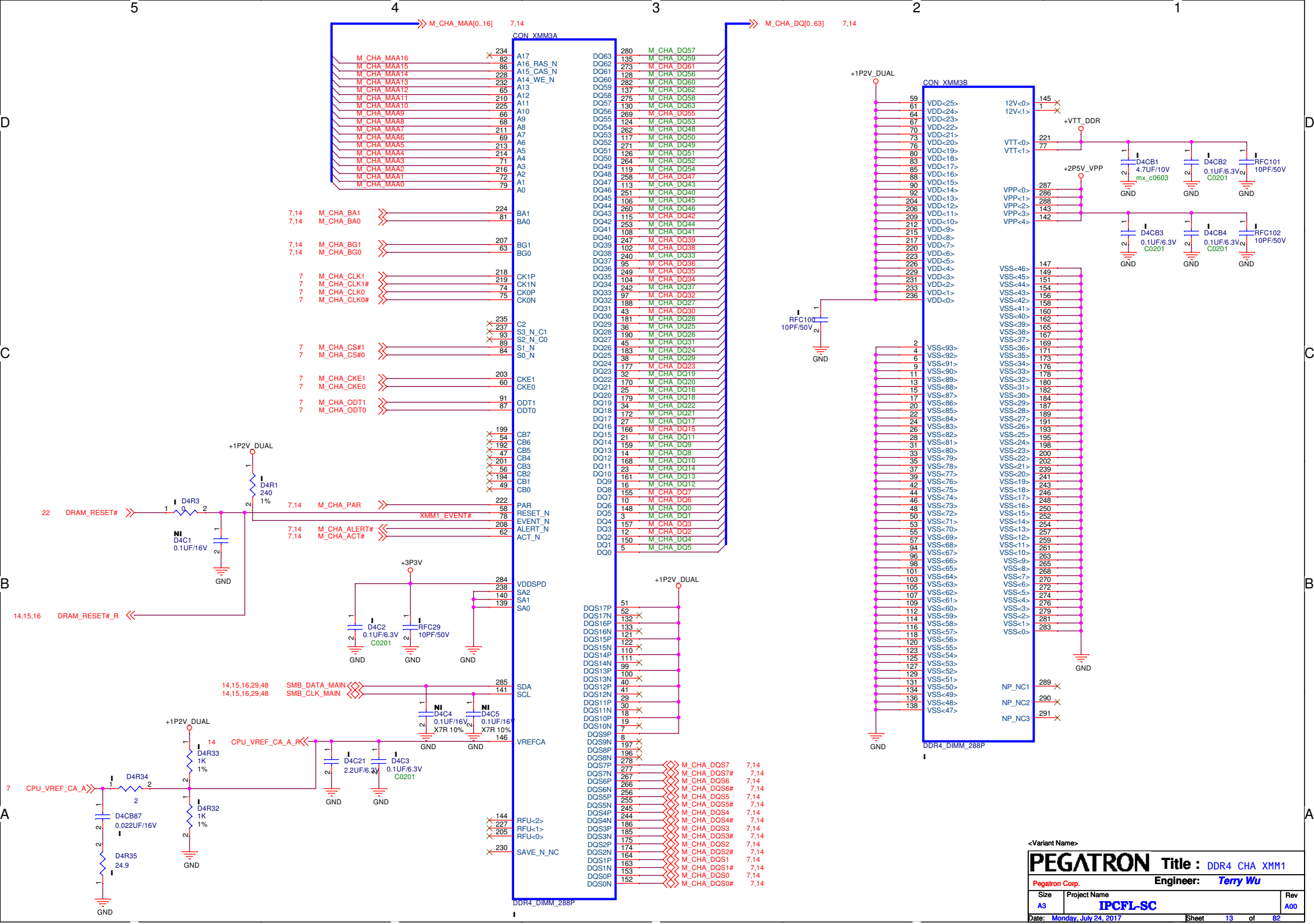
Size	Project Name	Rev
A3	IPCFL-SC	A00

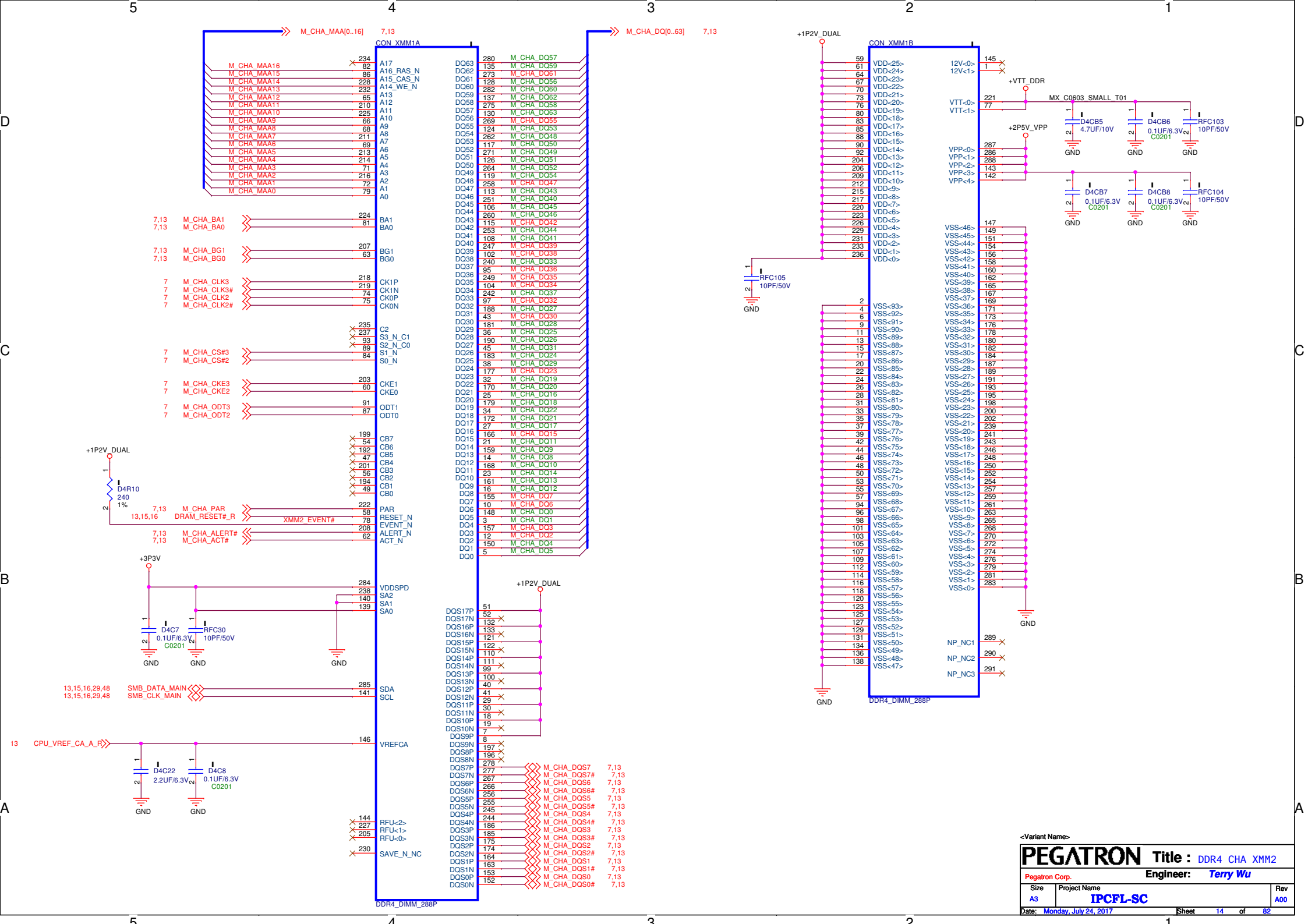
Date: Monday, July 24, 2017 Sheet 9 of 86

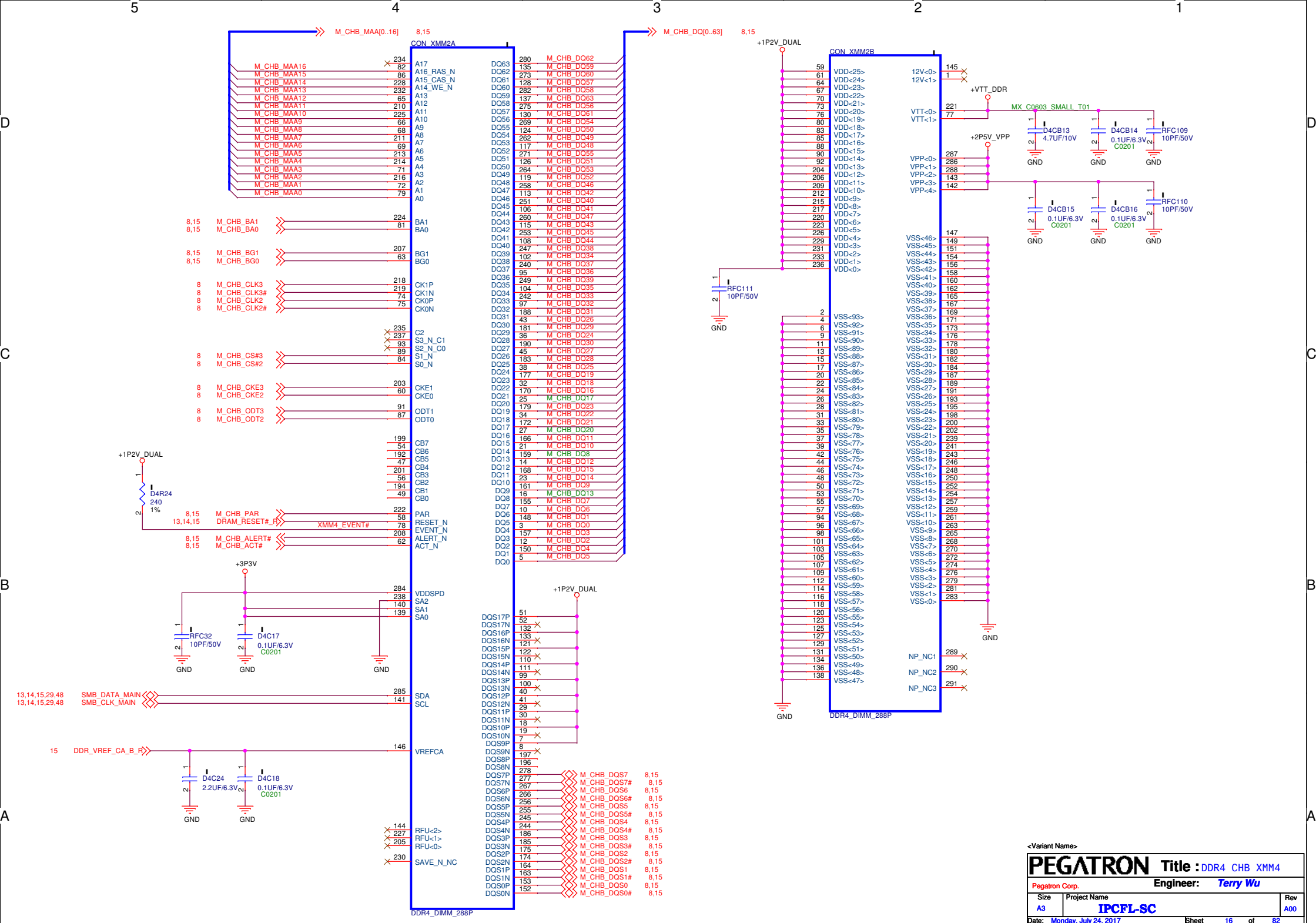














SATA HDD1

45 SATA_TXP0
45 SATA_TXN0
45 SATA_RXP0
45 SATA_RXN0

SATA HDD2

45 SATA_TXP1
45 SATA_TXN1
45 SATA_RXP1
45 SATA_RXN1

SATA HDD3

45 SATA_TXP2
45 SATA_TXN2
45 SATA_RXP2
45 SATA_RXN2

SATA HDD4

45 SATA_TXP3
45 SATA_TXN3
45 SATA_RXP3
45 SATA_RXN3

M.2 Key M slot

32 PE17_TXP
32 PE17_TXN
32 PE17_RXP
32 PE17_RXN

32 PE18_TXP
32 PE18_TXN
32 PE18_RXP
32 PE18_RXN

32 PE19_TXP
32 PE19_TXN
32 PE19_RXP
32 PE19_RXN

32 PE20_TXP
32 PE20_TXN
32 PE20_RXP
32 PE20_RXN

PCHB

PCIE/SATA

B36 PCIE13_TXP/SATA0B_TXP
C38 PCIE13_TXN/SATA0B_TXN
E35 PCIE13_RXP/SATA0B_RXP
G35 PCIE13_RXN/SATA0B_RXN

B37 PCIE14_TXP/SATA1B_TXP
A37 PCIE14_TXN/SATA1B_TXN
G37 PCIE14_RXP/SATA1B_RXP
E37 PCIE14_RXN/SATA1B_RXN

B38 PCIE15_TXP/SATA2_TXP
C38 PCIE15_TXN/SATA2_TXN
C42 PCIE15_RXP/SATA2_RXP
E41 PCIE15_RXN/SATA2_RXN

A39 PCIE16_TXP/SATA3_TXP
B39 PCIE16_TXN/SATA3_TXN
E43 PCIE16_RXP/SATA3_RXP
D42 PCIE16_RXN/SATA3_RXN

F45 PCIE17_TXP/SATA4_TXP
E45 PCIE17_TXN/SATA4_TXN
K39 PCIE17_RXP/SATA4_RXP
J41 PCIE17_RXN/SATA4_RXN

G44 PCIE18_TXP/SATA5_TXP
G45 PCIE18_TXN/SATA5_TXN
M41 PCIE18_RXP/SATA5_RXP
M39 PCIE18_RXN/SATA5_RXN

H45 PCIE19_TXP/SATA6_TXP
H44 PCIE19_TXN/SATA6_TXN
P41 PCIE19_RXP/SATA6_RXP
P39 PCIE19_RXN/SATA6_RXN

J44 PCIE20_TXP/SATA7_TXP
J43 PCIE20_TXN/SATA7_TXN
P36 PCIE20_RXP/SATA7_RXP
P38 PCIE20_RXN/SATA7_RXN

K44 PCIE_21_TXP
T41 PCIE_21_TXN
T39 PCIE_21_RXP
T39 PCIE_21_RXN

L44 PCIE_22_TXP
L43 PCIE_22_TXN
V36 PCIE_22_RXP
V36 PCIE_22_RXN

N45 PCIE_23_TXP
N44 PCIE_23_TXN
V41 PCIE_23_RXP
V39 PCIE_23_RXN

P44 PCIE_24_TXP
Y41 PCIE_24_TXN
Y39 PCIE_24_RXP
Y39 PCIE_24_RXN

AF44 GPP_F5/DEVSLP3
AG41 GPP_F6/DEVSLP4
AH39 GPP_F7/DEVSLP5
AH36 GPP_F8/DEVSLP6
AF45 GPP_F9/DEVSLP7

AE30 GPP_F10/SCLOCK
AH35 GPP_F11/SLOAD
AE44 GPP_F12/SDATAOUT1
AE43 GPP_F13/SDATAOUT0
AD44 GPP_F14

AC42 GPP_F19/6DP_VDDEN
AE35 GPP_F20/6DP_BKLTEN
AE36 GPP_F21/6DP_BKLTCTL

AB45 GPP_F22
AE39 GPP_F23

GPP_E0/SATAXPCIE0/SATAGP0
GPP_E1/SATAXPCIE1/SATAGP1
GPP_E2/SATAXPCIE2/SATAGP2

GPP_E3/CPU_GP0
GPP_E4/DEVSLP0
GPP_E5/DEVSLP1
GPP_E6/DEVSLP2
GPP_E7/CPU_GP1
GPP_E8/SATALED#

GPP_E9/USB_OC0#
GPP_E10/USB_OC1#
GPP_E11/USB_OC2#
GPP_E12/USB_OC3#

GPP_F15/USB_OCB4#
GPP_F16/USB_OCB5#
GPP_F17/USB_OCB6#
GPP_F18/USB_OC7#

GPP_I0/DDPB_HPD0
GPP_I1/DDPC_HPD1
GPP_I2/DDPD_HPD2
GPP_I3/DDPE_HPD3
GPP_I4/EDP_HPD

GPP_I5/DDPB_CTRLCLK
GPP_I6/DDPB_CTRLDATA
GPP_I7/DDPC_CTRLCLK
GPP_I8/DDPC_CTRLDATA
GPP_I9/DDPD_CTRLCLK
GPP_I10/DDPD_CTRLDATA

GPP_F0/SATAXPCIE3/SATAGP3
GPP_F1/SATAXPCIE4/SATAGP4
GPP_F2/SATAXPCIE5/SATAGP5
GPP_F3/SATAXPCIE6/SATAGP6
GPP_F4/SATAXPCIE7/SATAGP7

AM36
AM35
AM36

AP41
AL44
AL45
AK44
AK43
AJ44

AJ43
AH44
AM39
AK42

AD43
AC44
AH42
AC43

AP7
AT8
AP8
AT7
BA1

AW5
AV7
AT5
BA6
AY1
AY2

AK36
AK33
AK38
AH43
AE42

+3P3V

SR94

10K

1%

MF_MODE#

HD_LED#

50

NI

FC8

0.1UF/16V

X7R 10%

GND

+3P3VSB

SR129

10K

USB_OC0#

80

USB_OC1#

80

USB_OC2#

44

USB_OC3#

42

USB_OCB4#

79

USB_OCB5#

41

OC_ASM1142_PA#

36,42

ASM1142_SMI#

36

DDPD_HPD

47

PCH_DDPD_CTRLCLK

46

PCH_DDPD_CTRLDATA

46

SATA2_PCIE3_DET

32

OC Signal	USB3.0	USB2.0	Power
USB_OC0#	U3_PORT1	U2_PORT7	+5V_Charger_1
USB_OC1#	U3_PORT2	U2_PORT13	+5V_Charger_2
USB_OC2#	U3_PORT3	U2_PORT9	+VCC_USB3_3
USB_OC2#	U3_PORT4	U2_PORT11	+VCC_USB3_3
USB_OC3#	U3_PORT6	U2_PORT10	+VCC_USB3_2
USB_OC3#	U3_PORT7	U2_PORT12	+VCC_USB3_2
USB_OCB4#	N/A	U2_PORT1	+VCC_USB2
USB_OCB4#	N/A	U2_PORT2	+VCC_USB2
USB_OCB4#	N/A	U2_PORT3	+VCC_USB2
USB_OCB4#	N/A	U2_PORT4	+VCC_USB2
USB_OCB5#	N/A	U2_PORT5	+VCC_USB2_1
USB_OCB5#	N/A	U2_PORT6	+VCC_USB2_1
USB_OC6#			

Version	Board_ID_D2	Board_ID_D1	Board_ID_D0
CFL_B00	0	0	0
CFL_X00	0	0	1
CFL_X01	0	1	0
CFL_X02	0	1	1
CFL_A00	1	0	0

KABYLAK_PCH

Rev 0.7

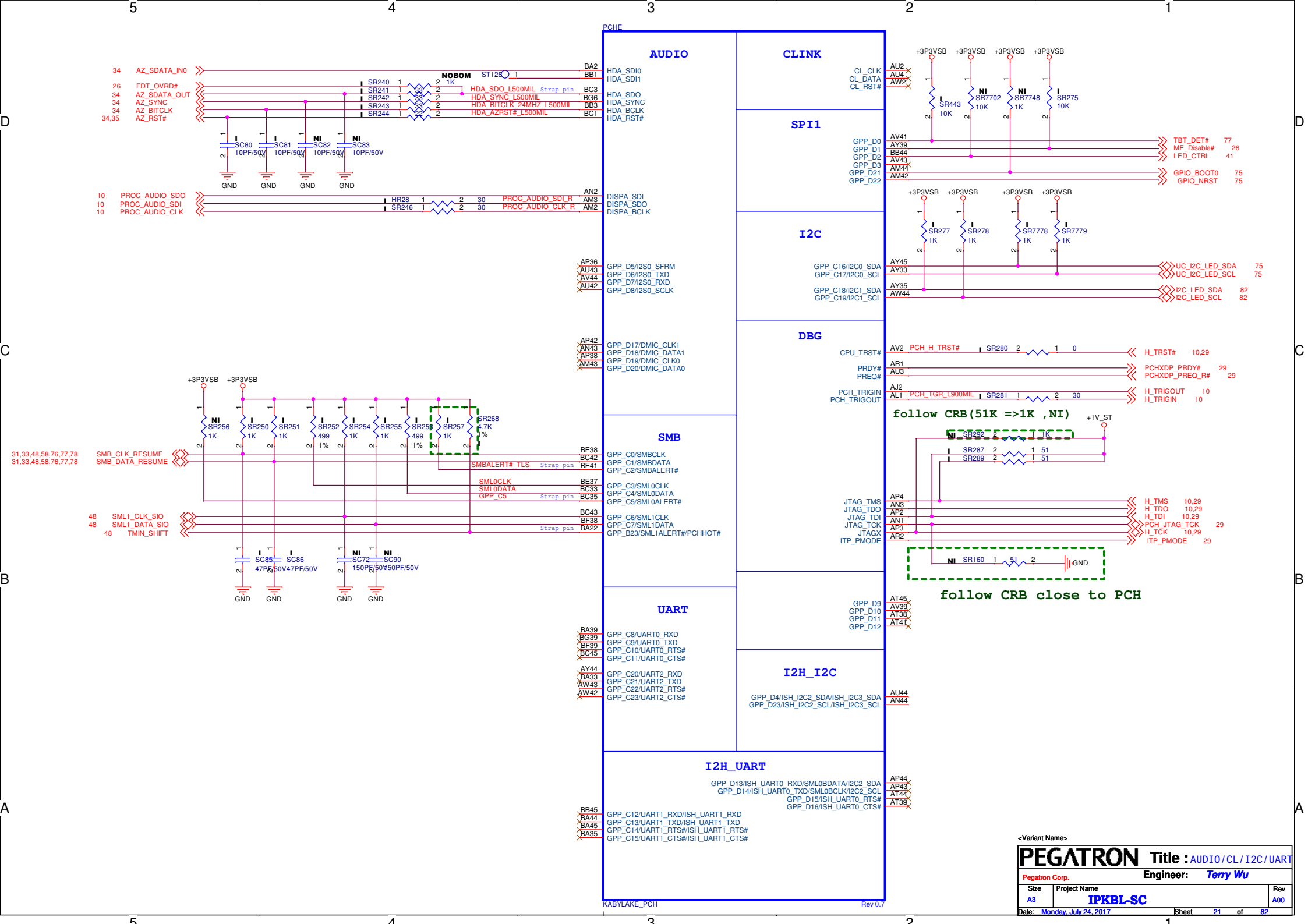
<Variant Name>

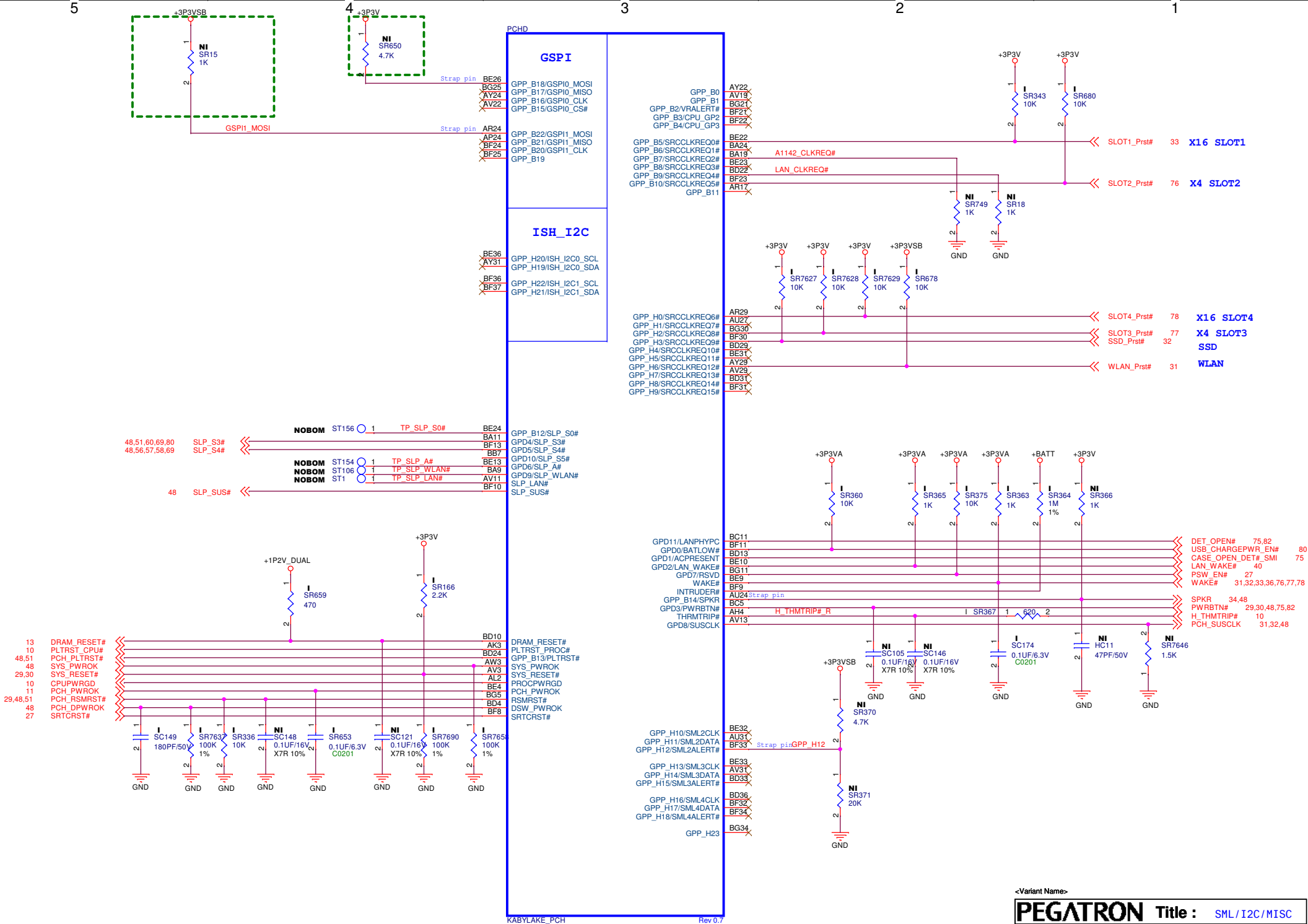
PEGATRON Title : SATA/PCIE

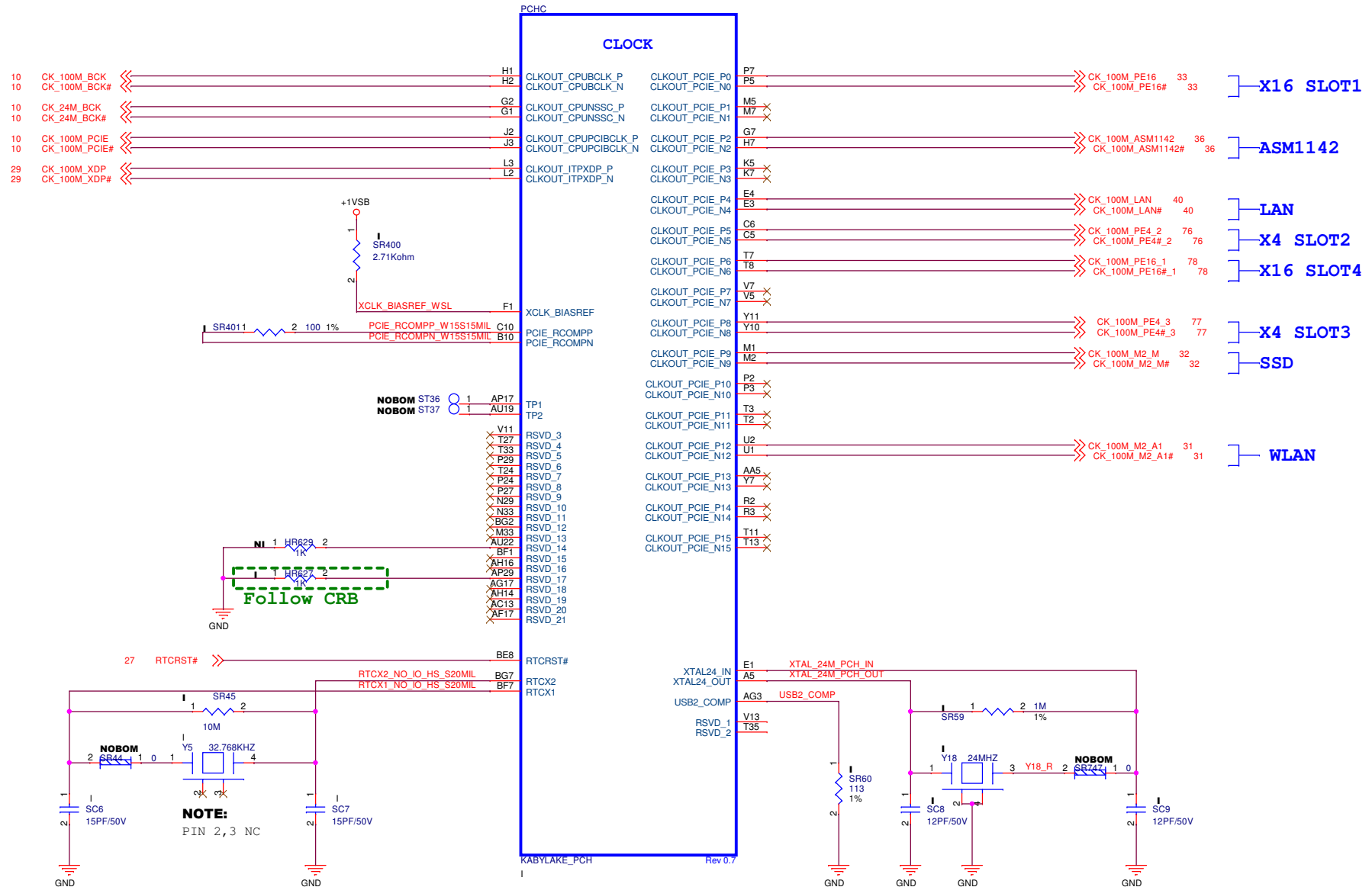
Pegatron Corp. Engineer: Terry Wu

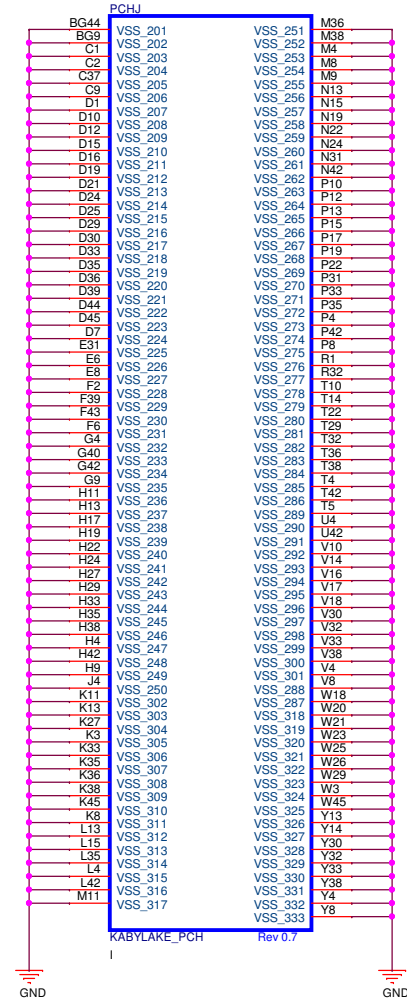
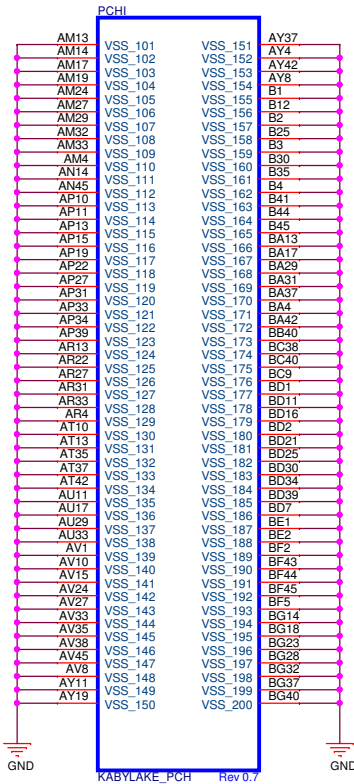
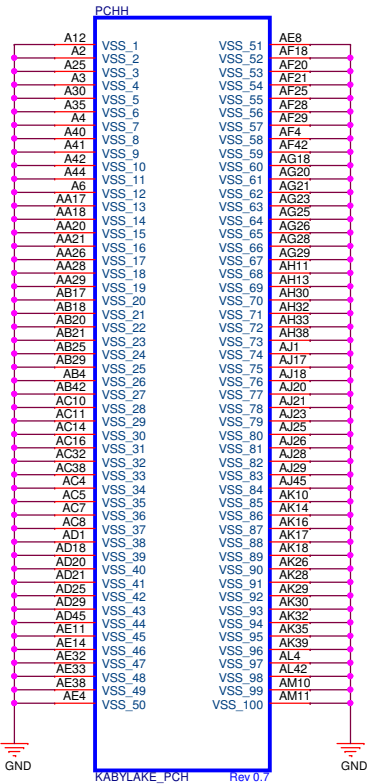
Size A3 Project Name IPKBL-SC Rev A00

Date: Monday, July 24, 2017 Sheet 19 of 82

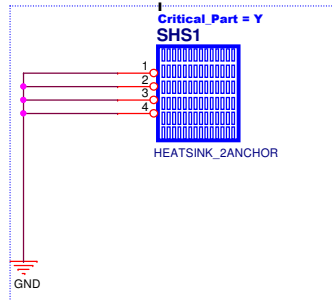




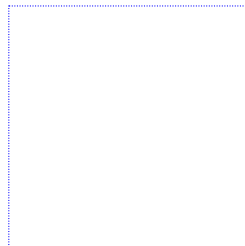




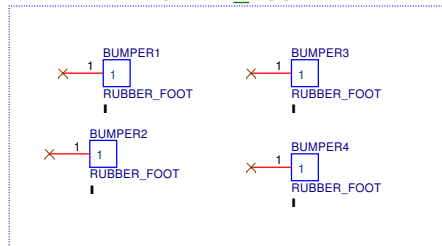
PCH Heatsinker



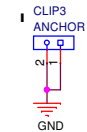
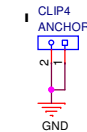
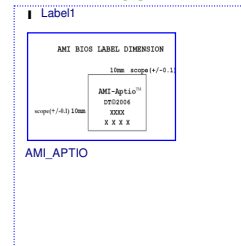
DELL PPID



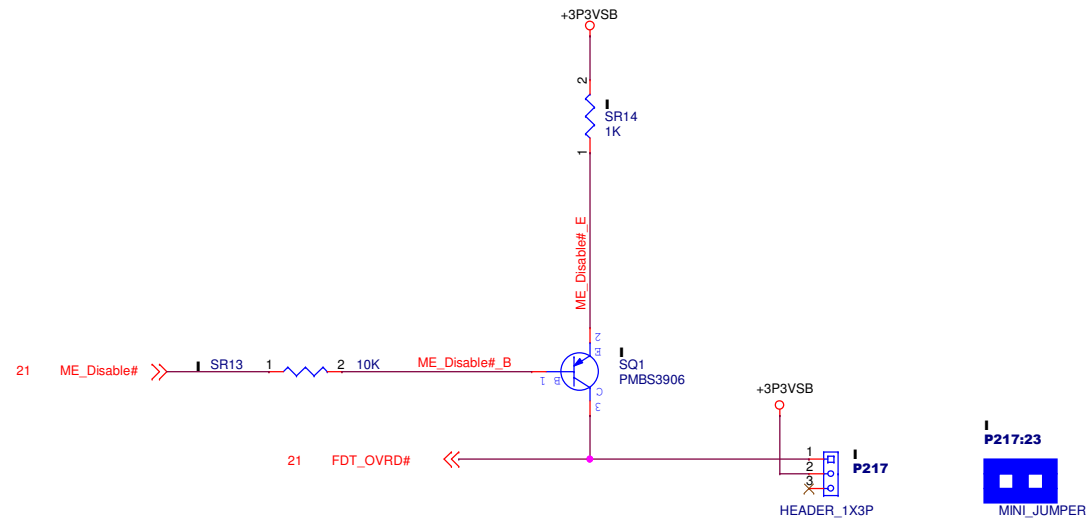
BUBBER_FOOT

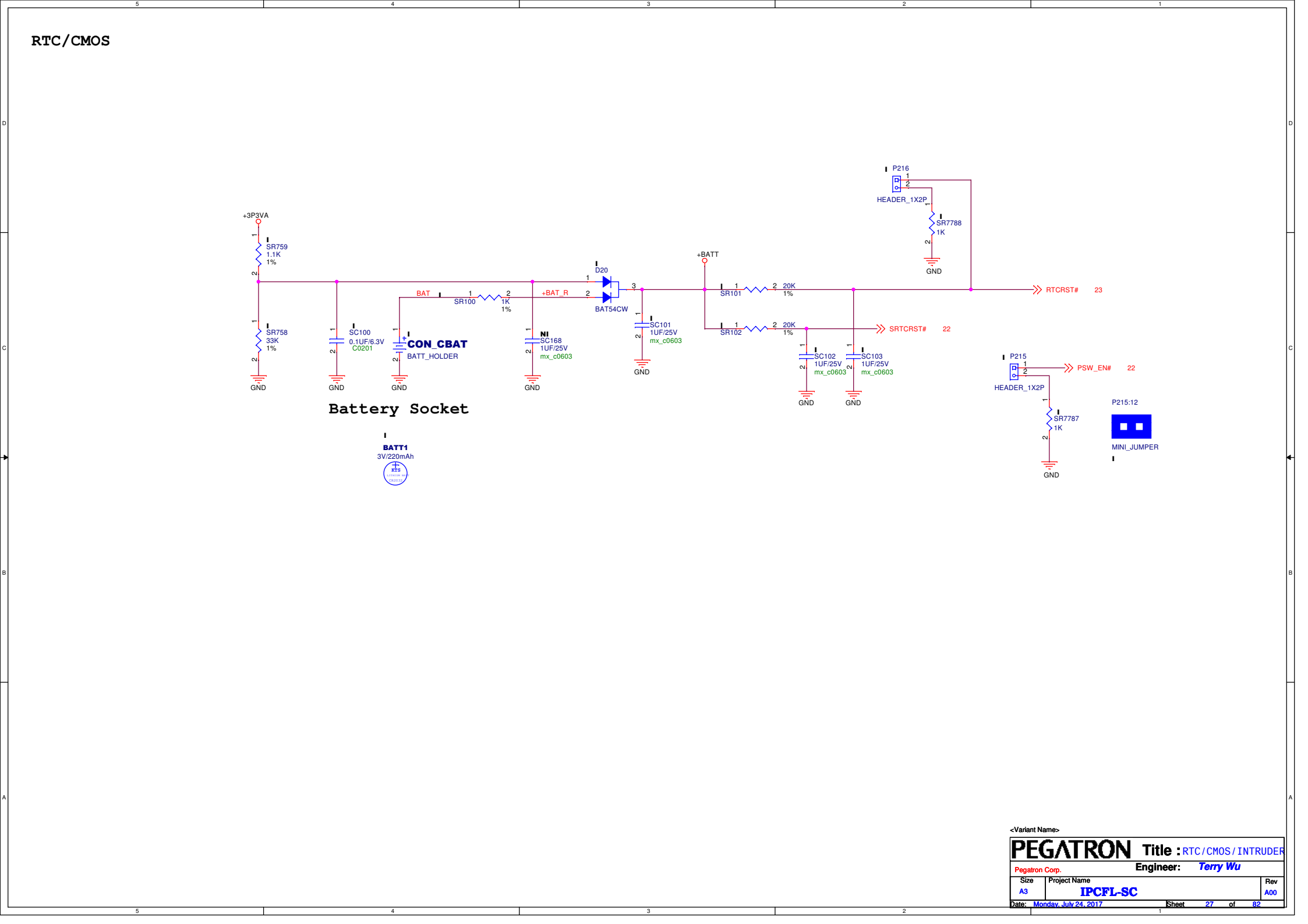


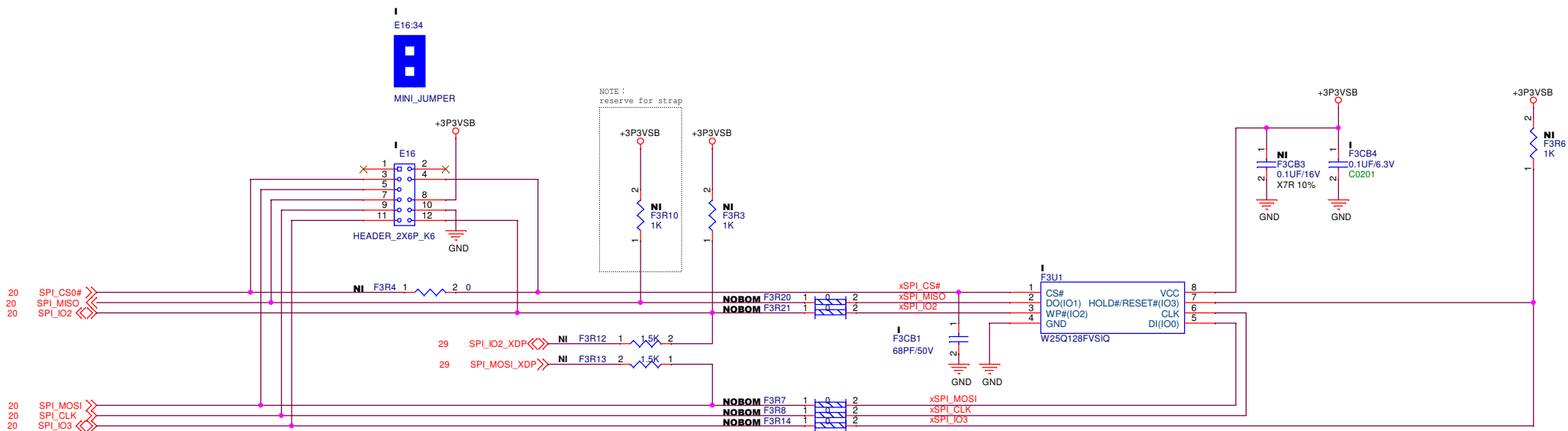
AMI BIOS LABEL

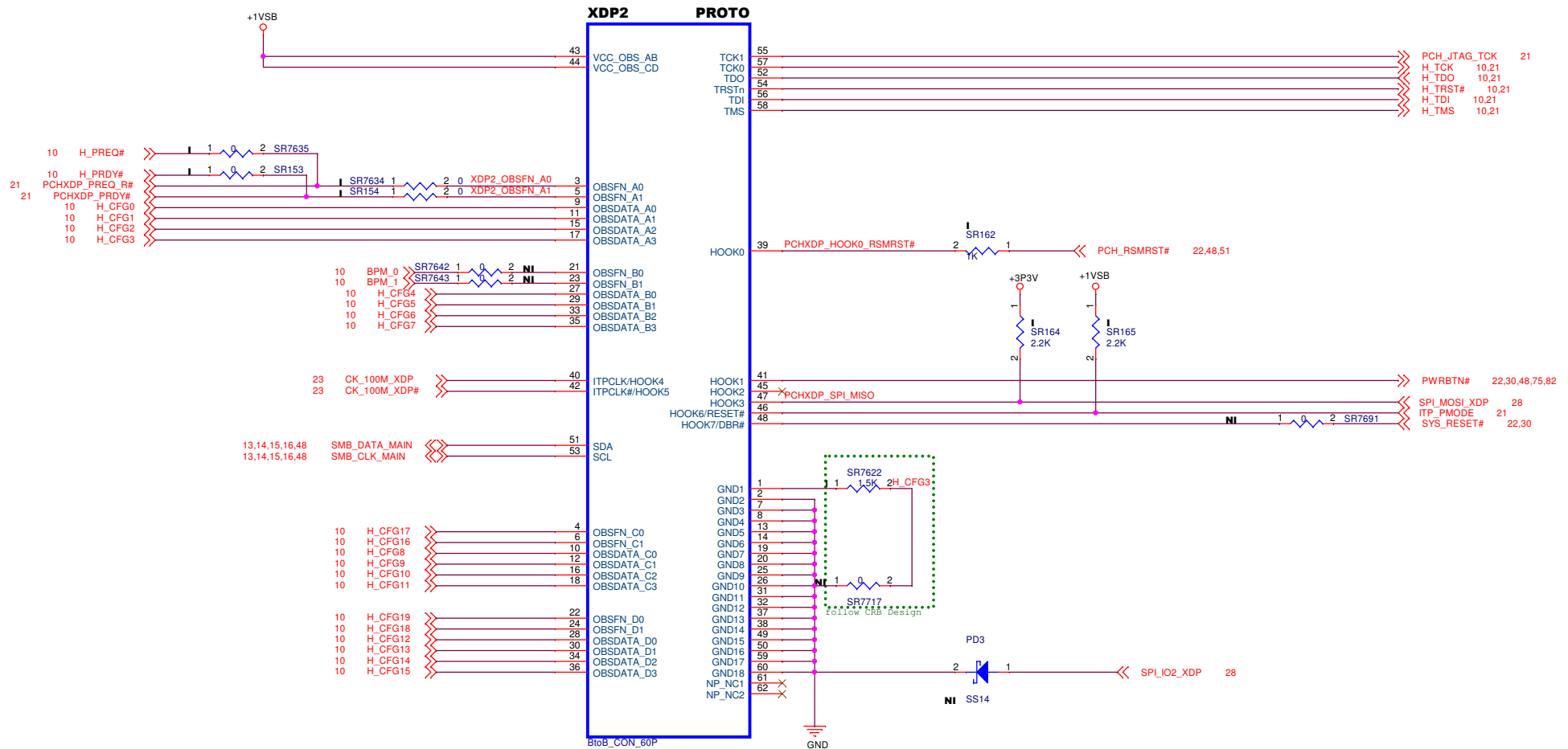


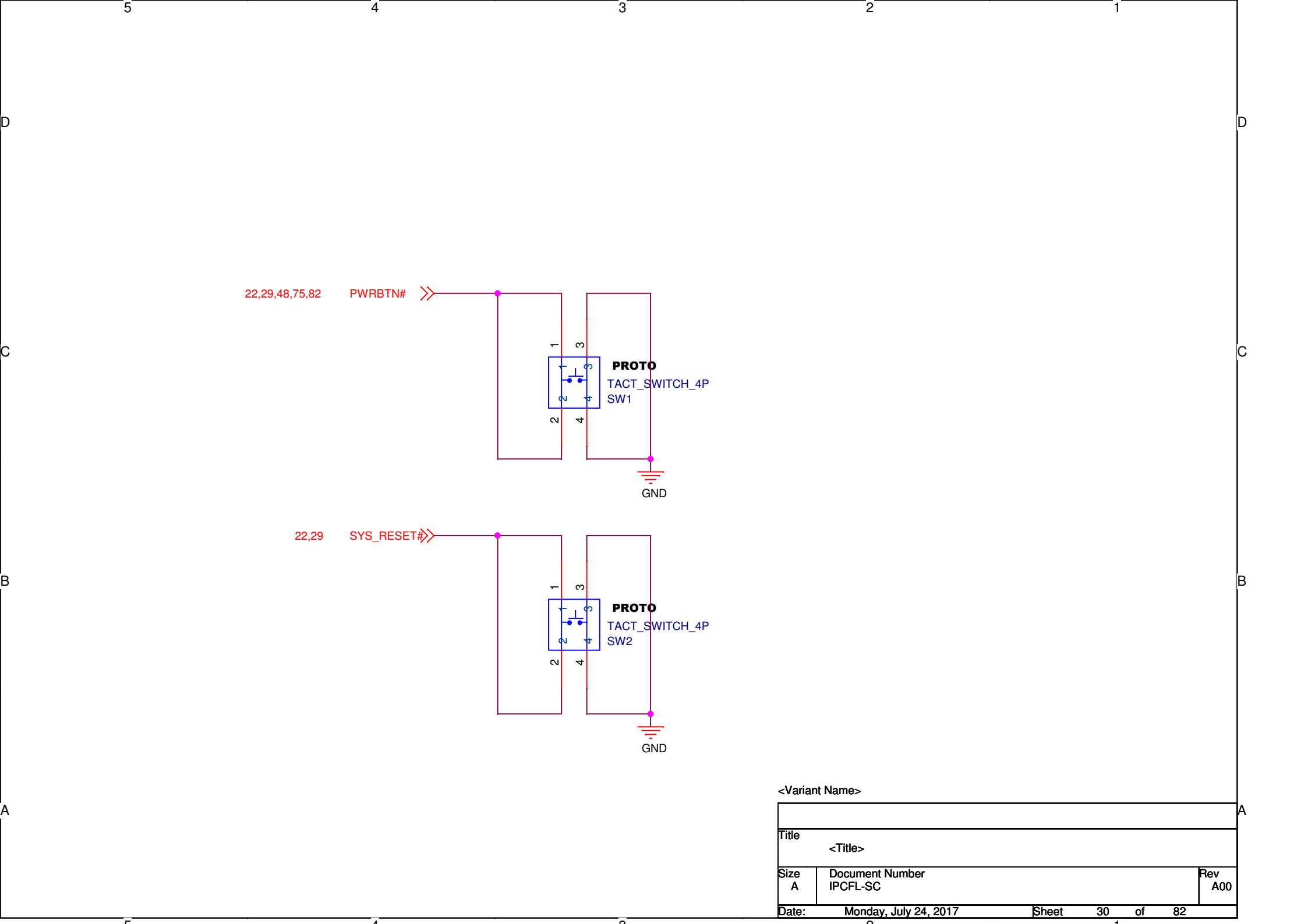
<Variant Name>

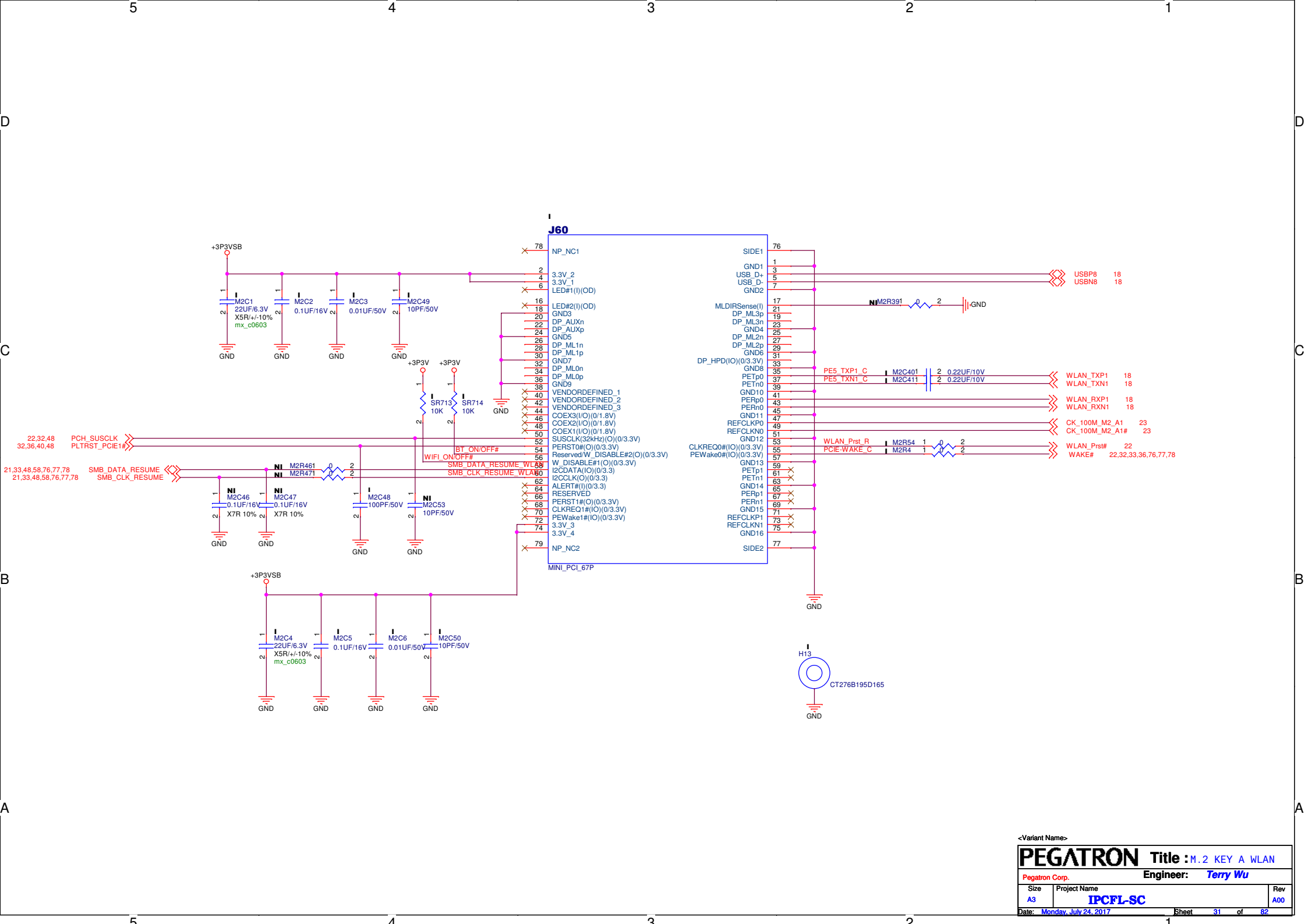


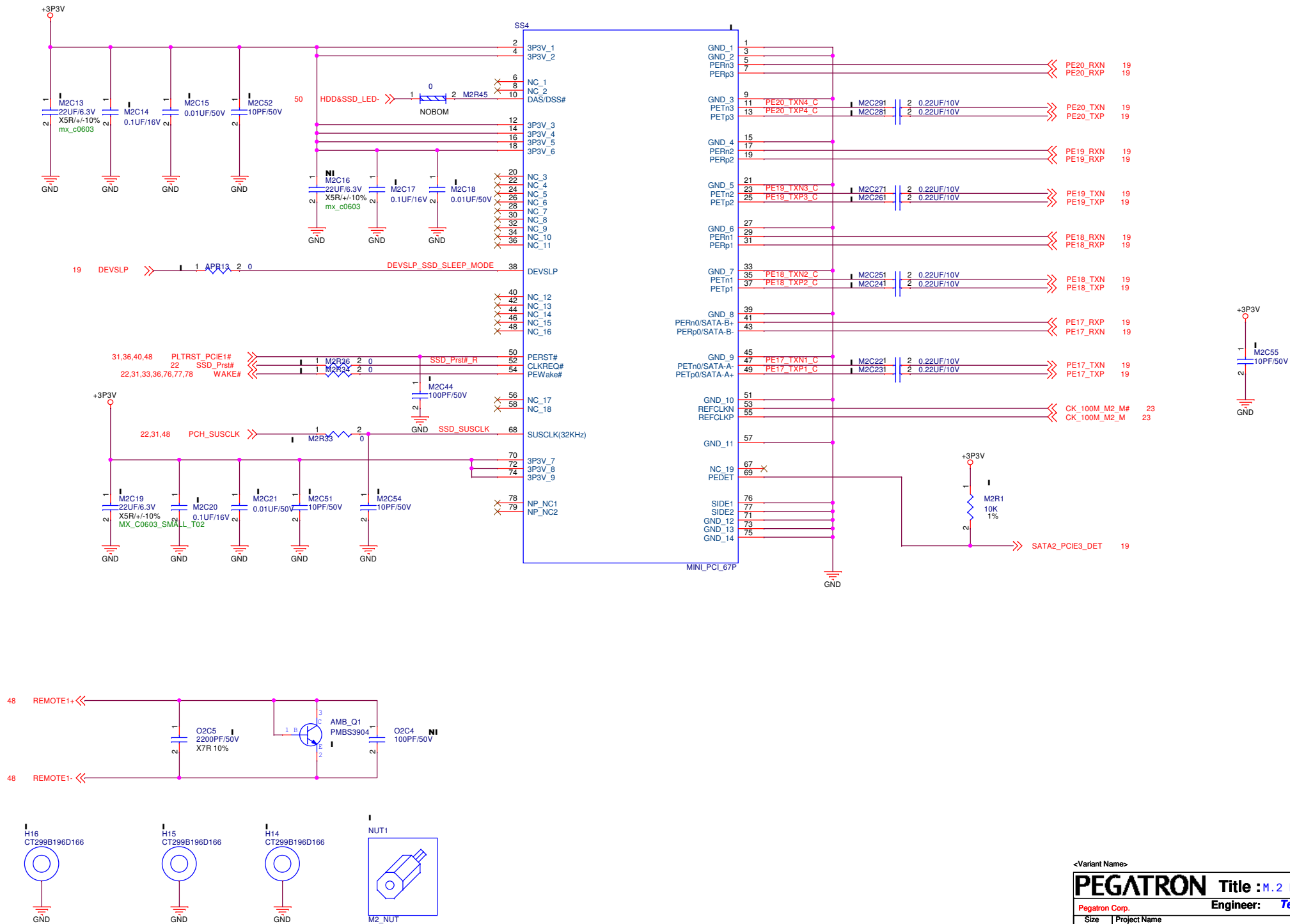






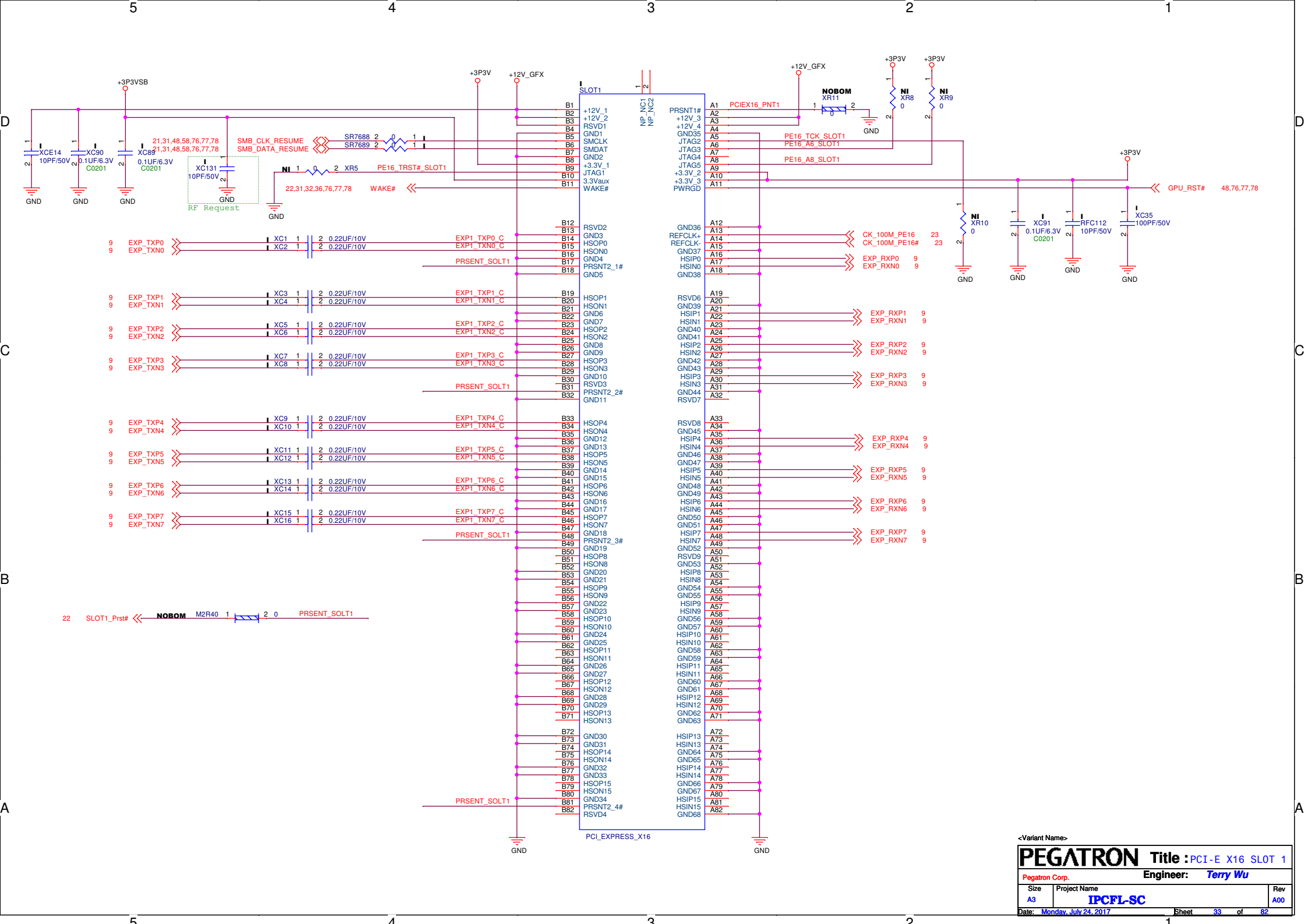


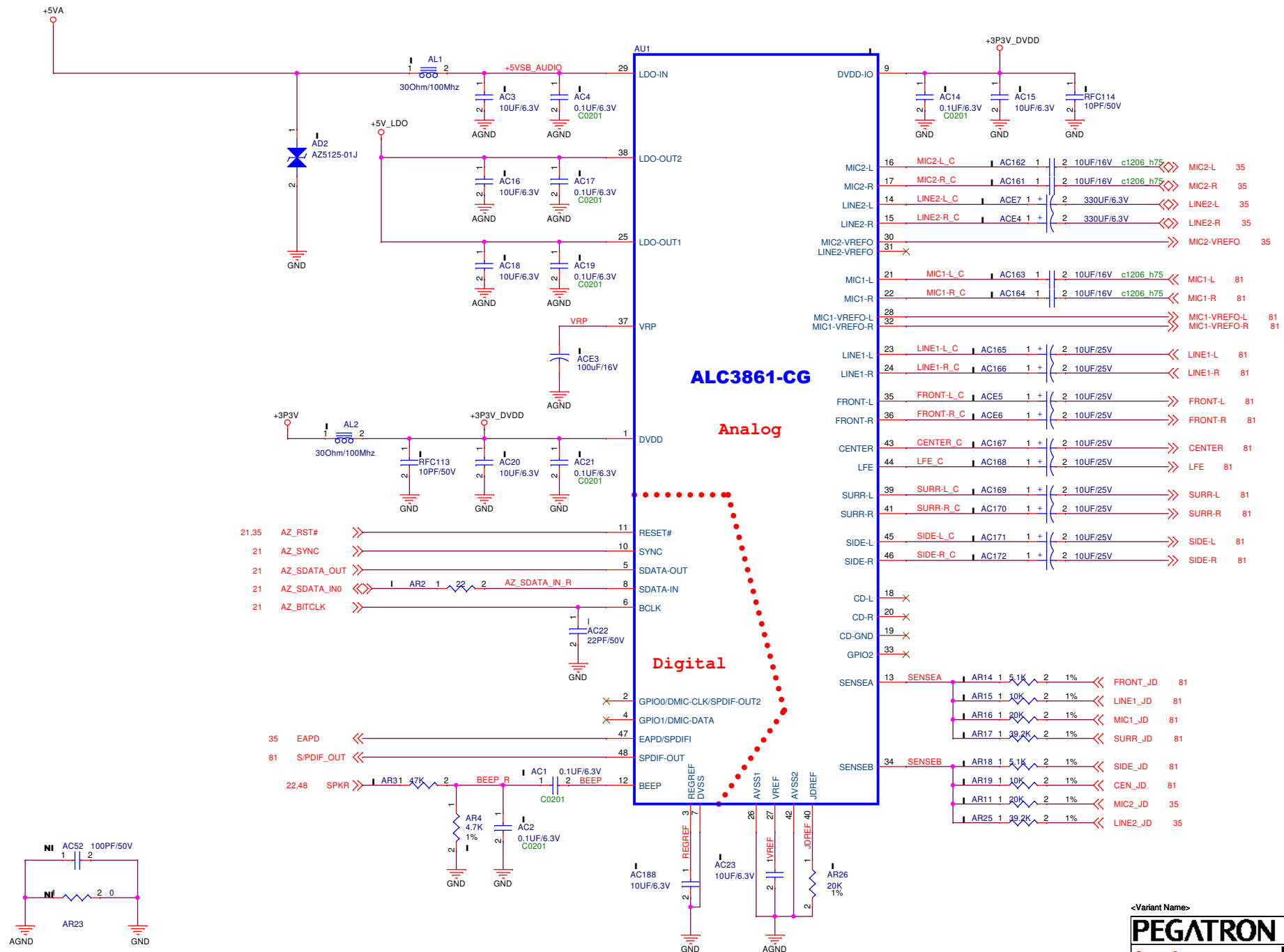


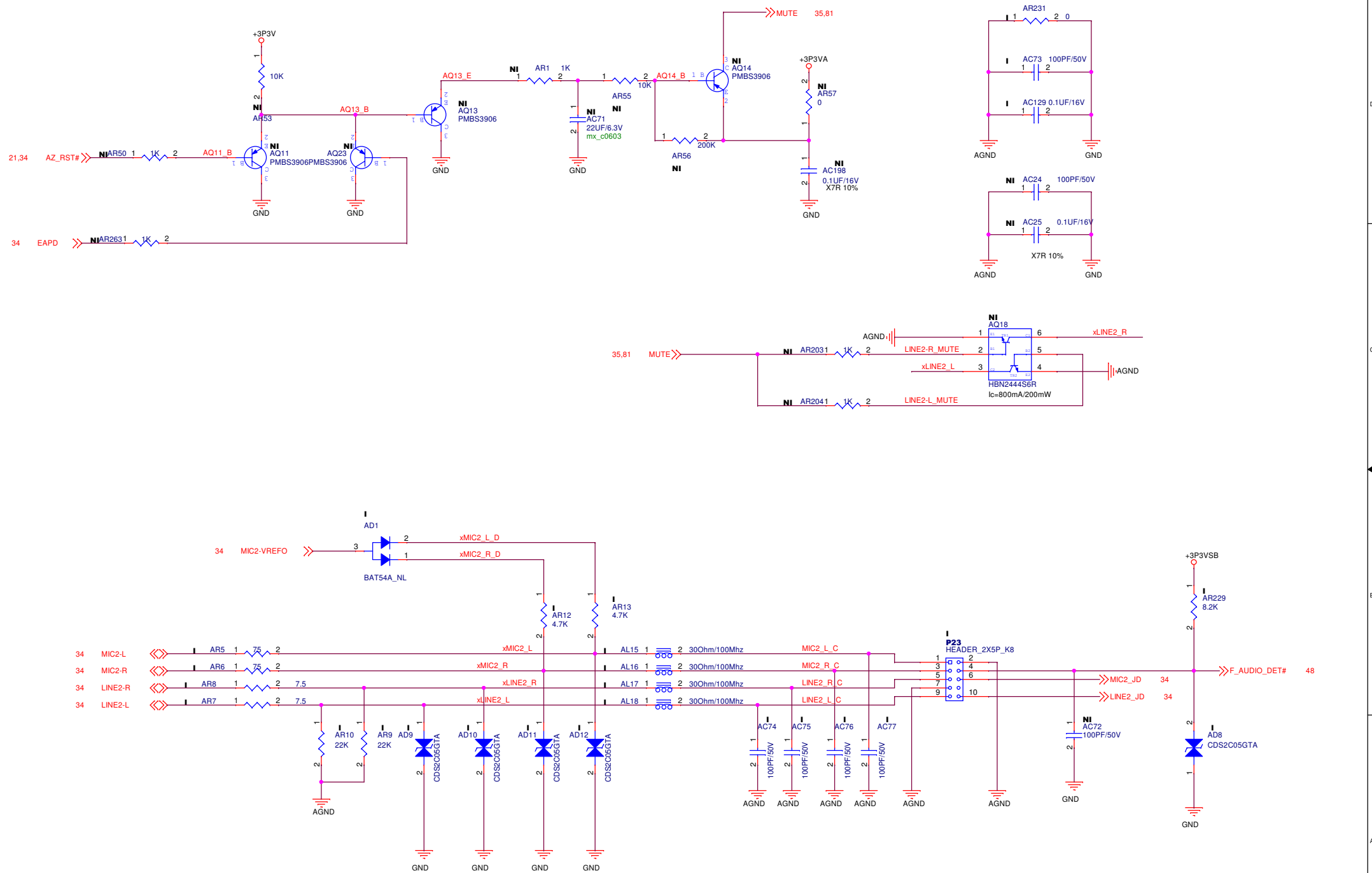


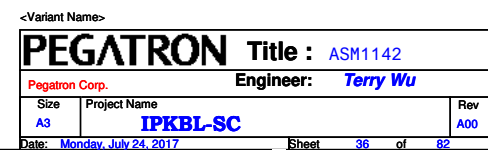
<Variant Name>

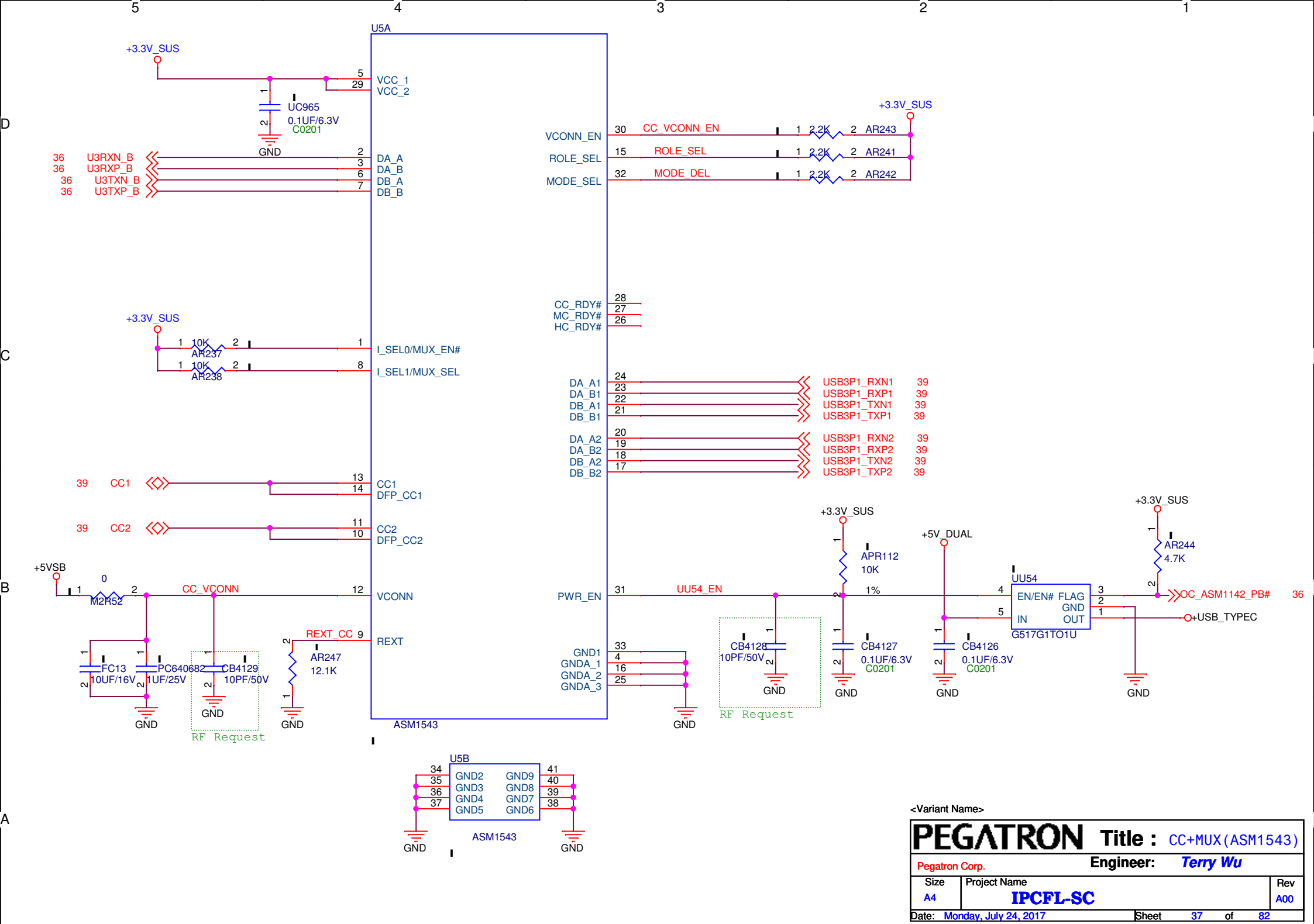
PEGATRON		Title : M.2 KEY M SSD	
Pegatron Corp.		Engineer: Terry Wu	
Size	Project Name	Rev	
A3	IPCFL-SC	A00	
Date: Monday, July 24, 2017		Sheet 32 of 82	













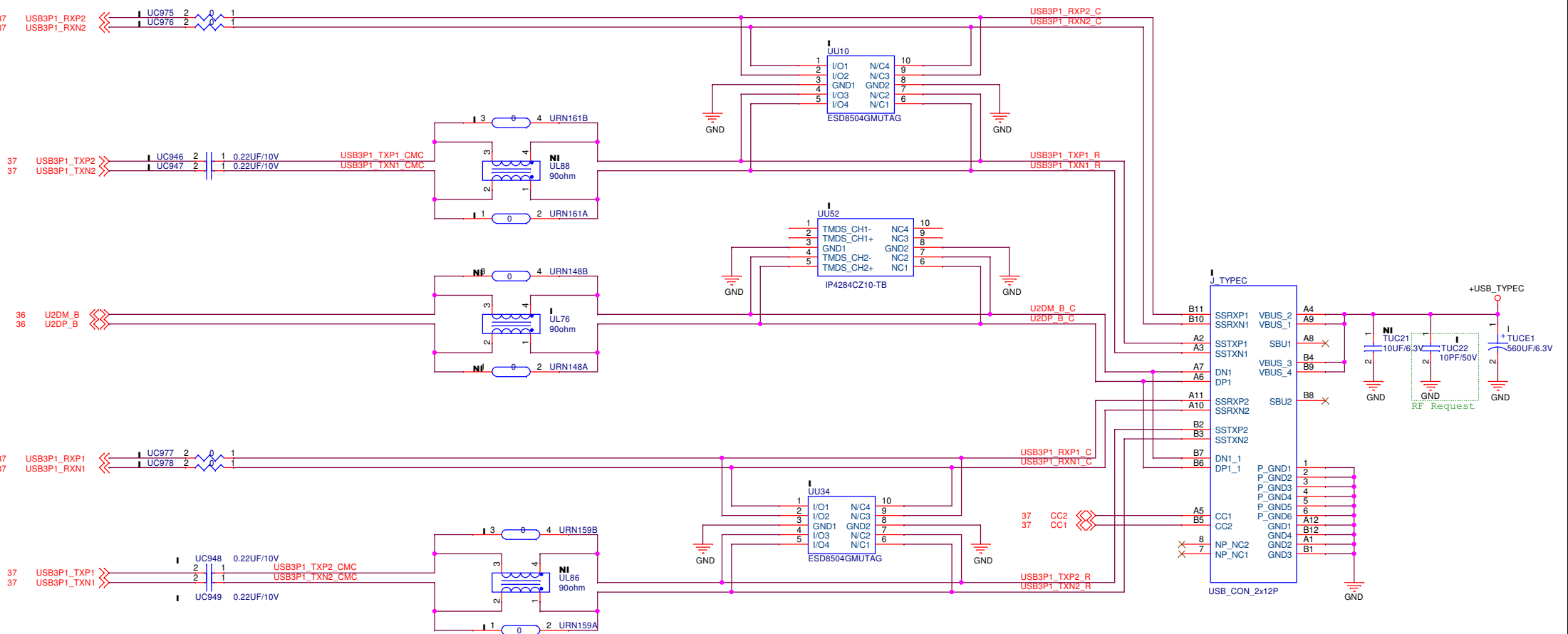
<Variant Name>

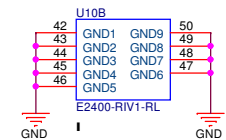
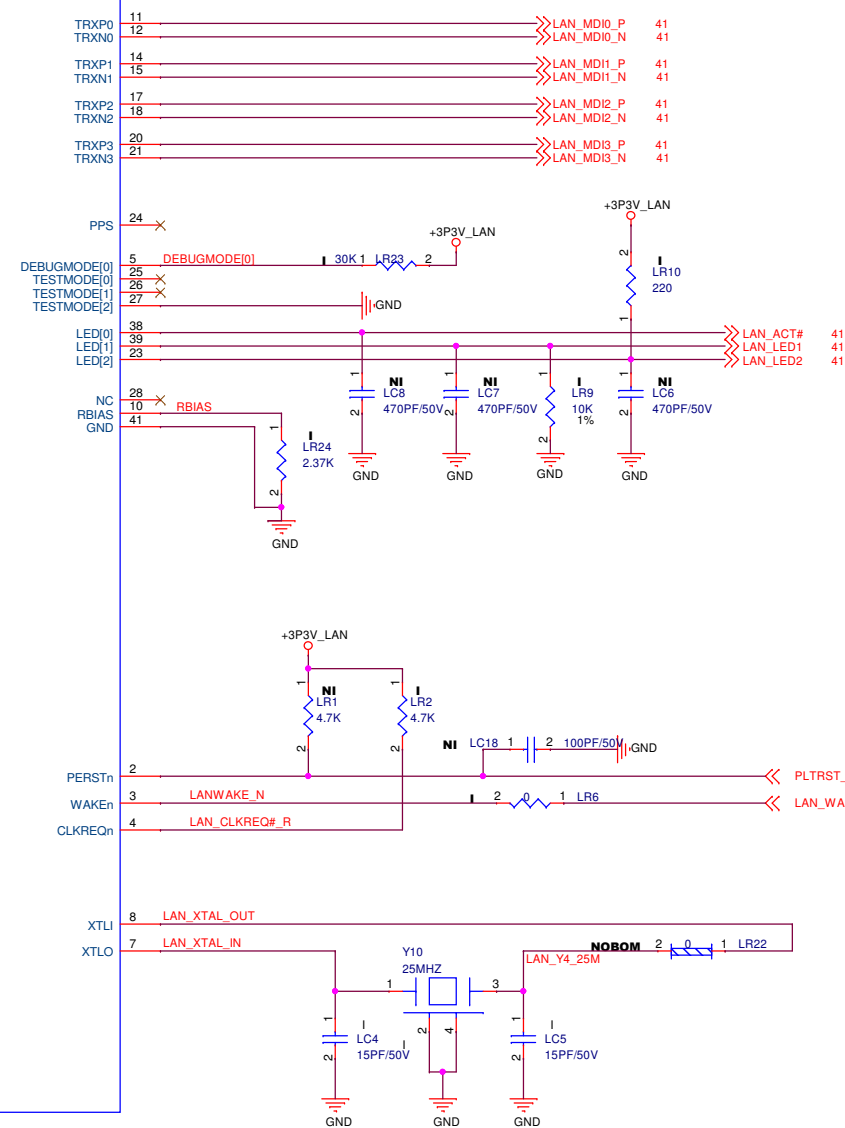
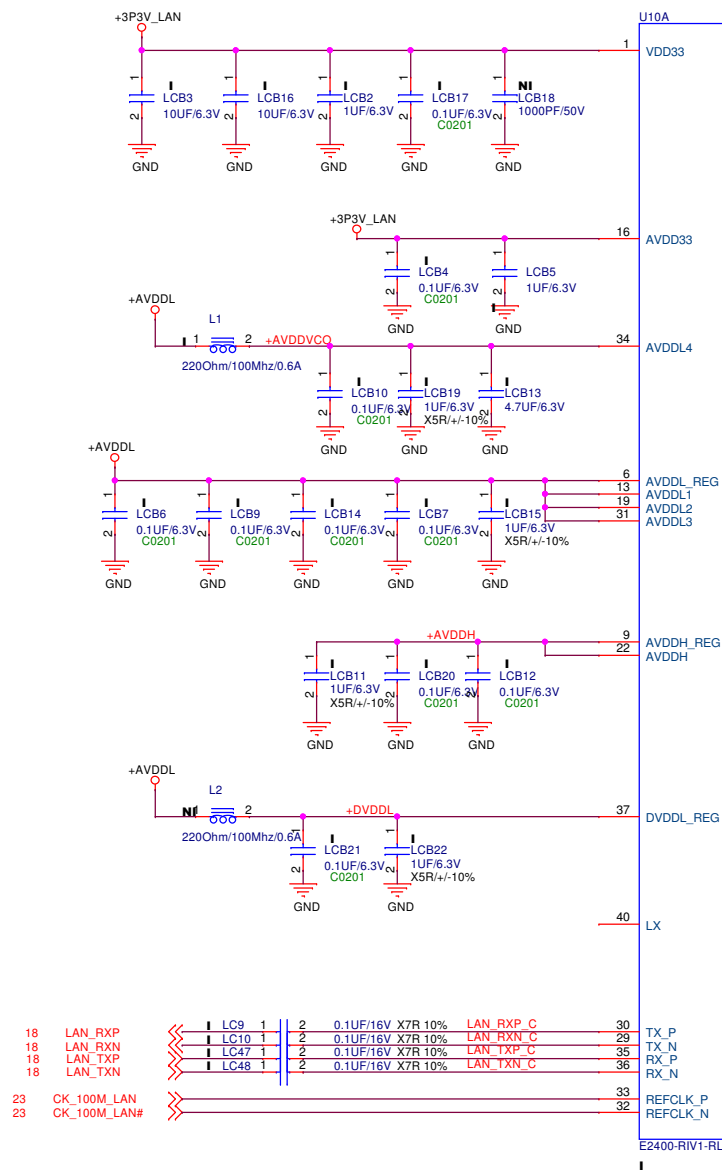
PEGATRON		Title : XXXX
Pegatron Corp.		Engineer: Terry Wu
Size A3	Project Name IPCFL-SC	Rev A00
Date: Monday, July 24, 2017		

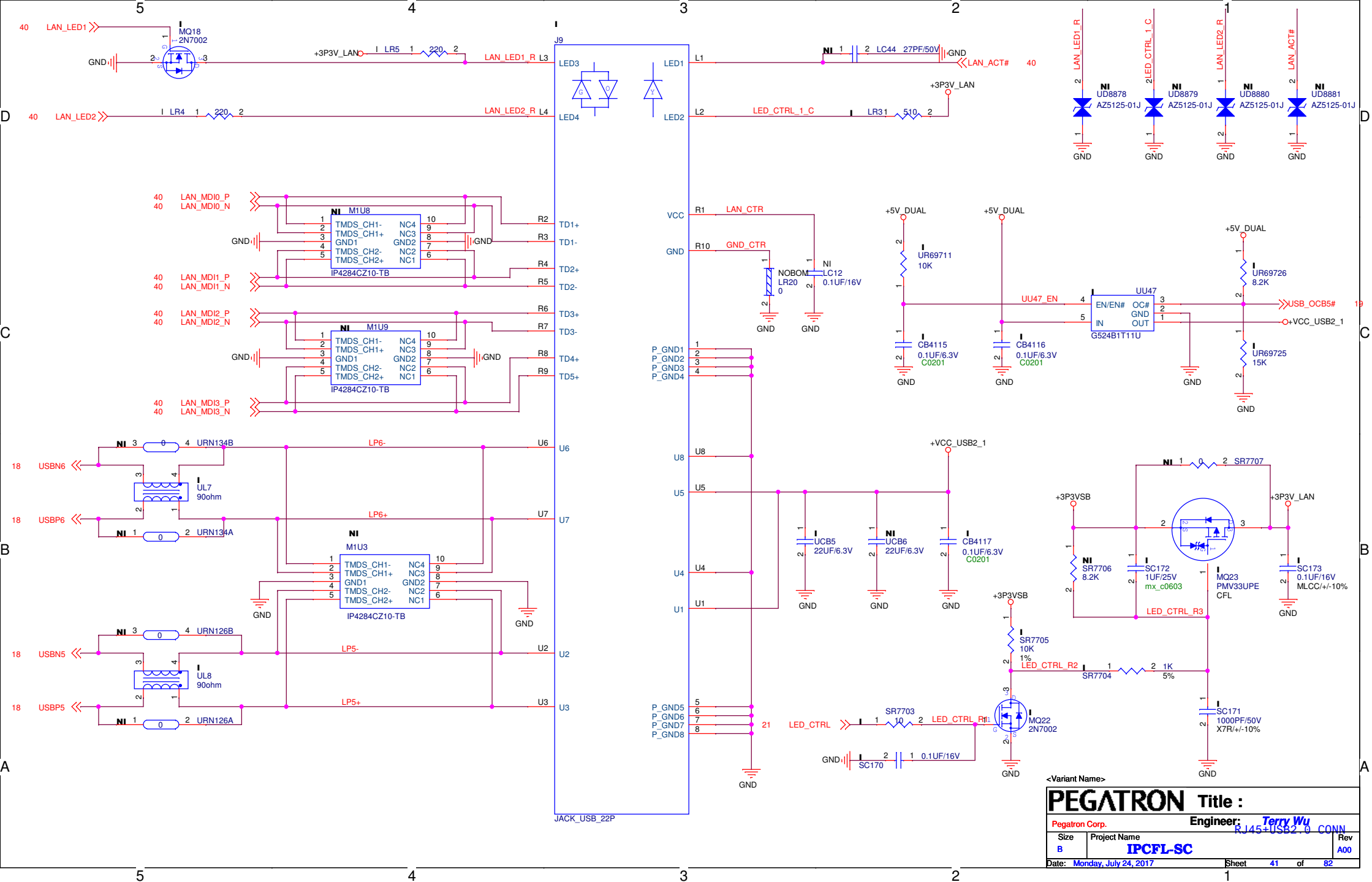
Sheet 38 of 82

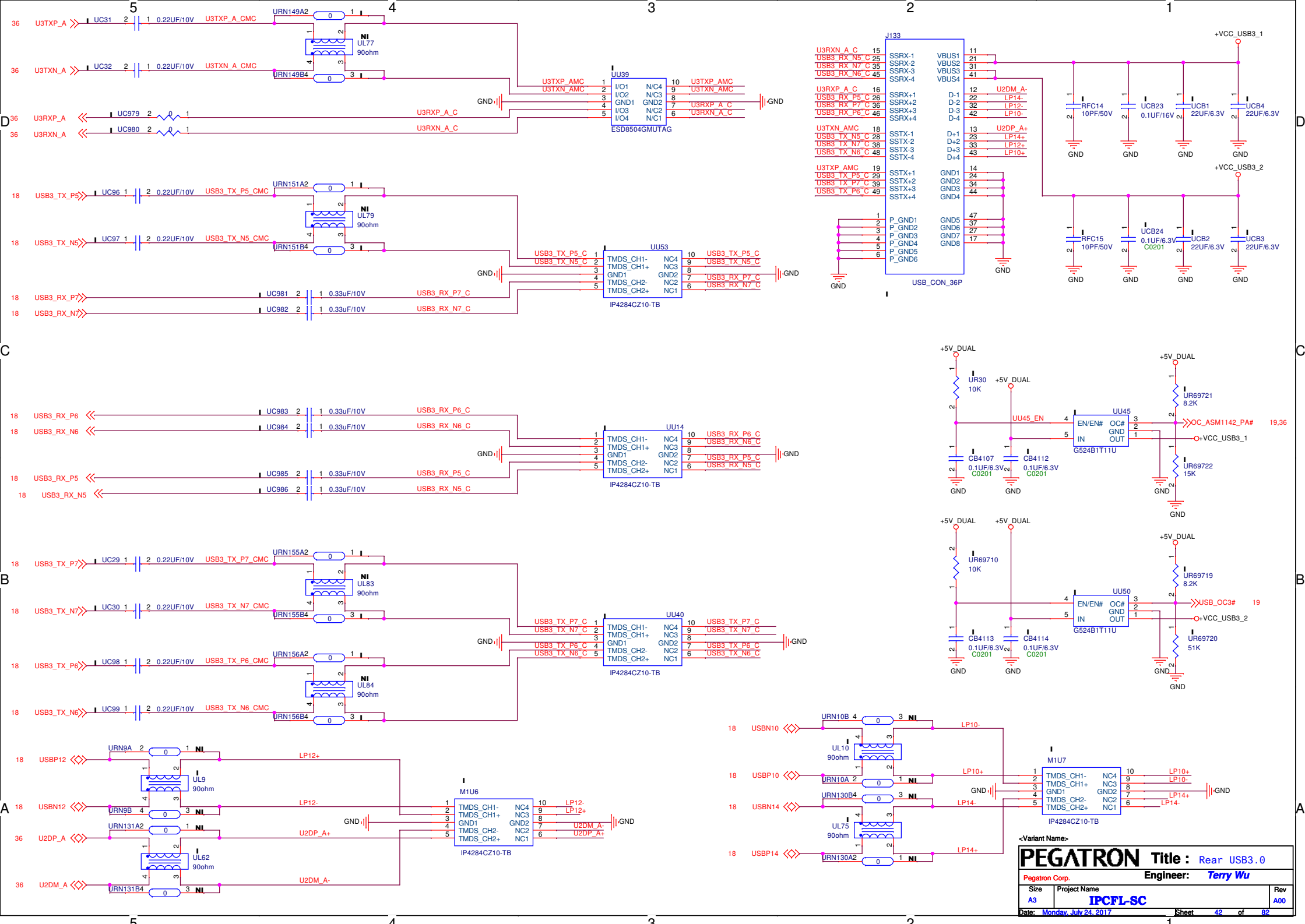
USB3.1(Type C) Pin define

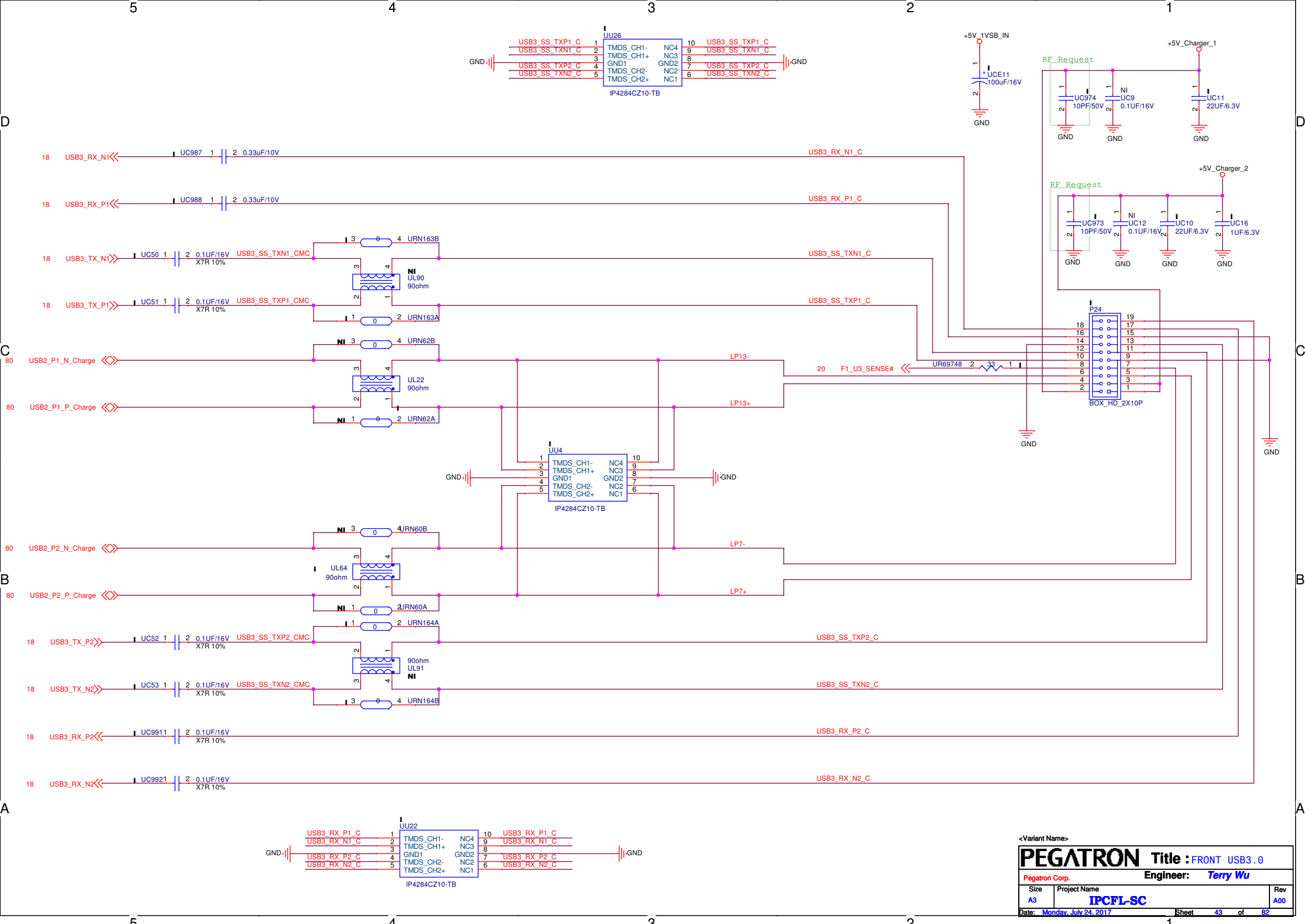
A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC1	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2	D-	D+	CC2	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

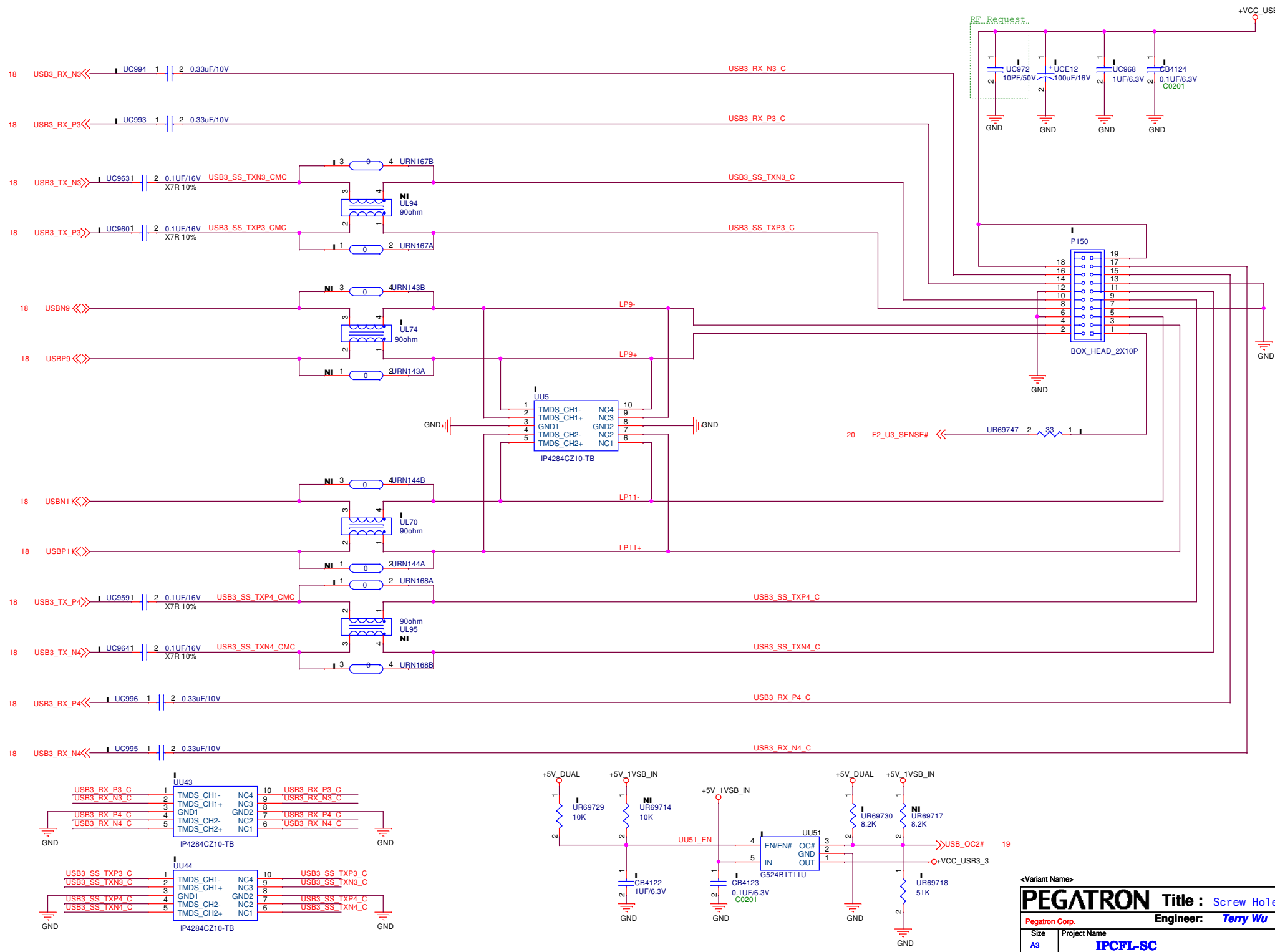


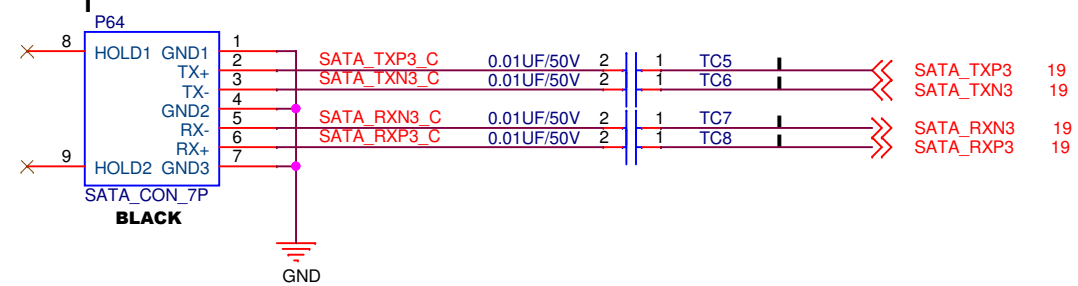
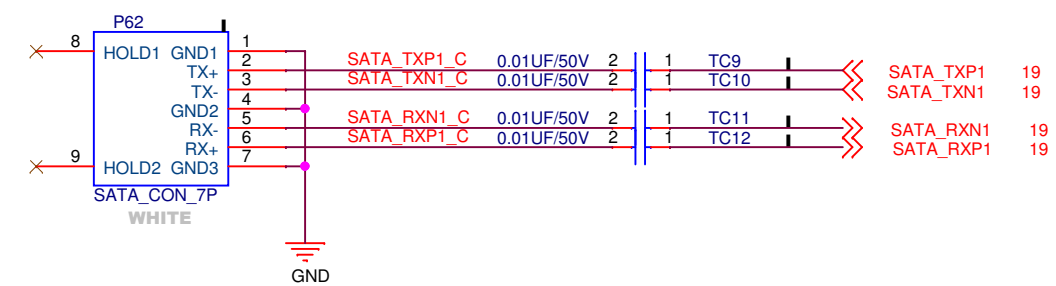
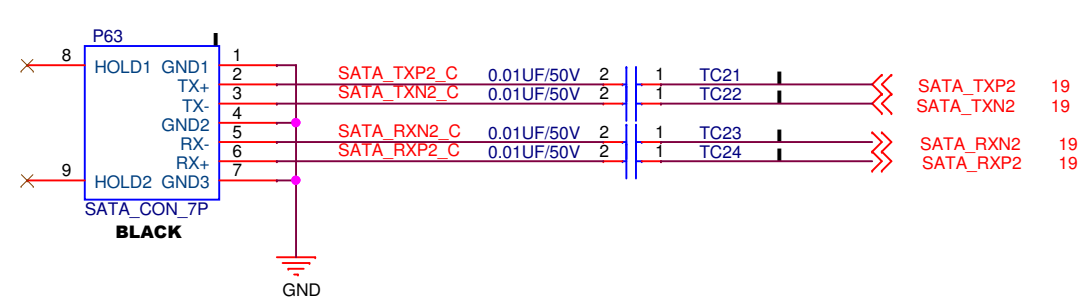
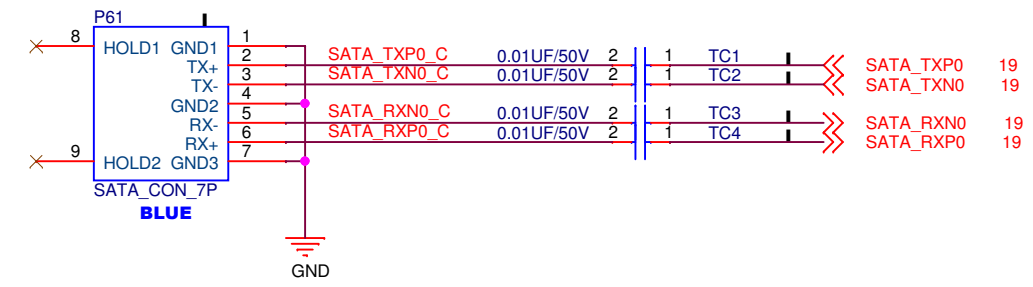


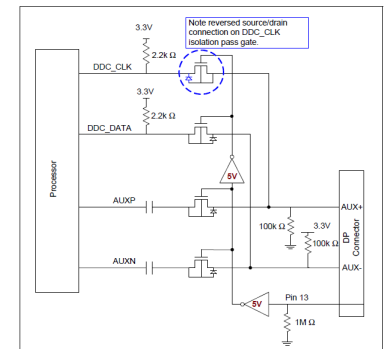
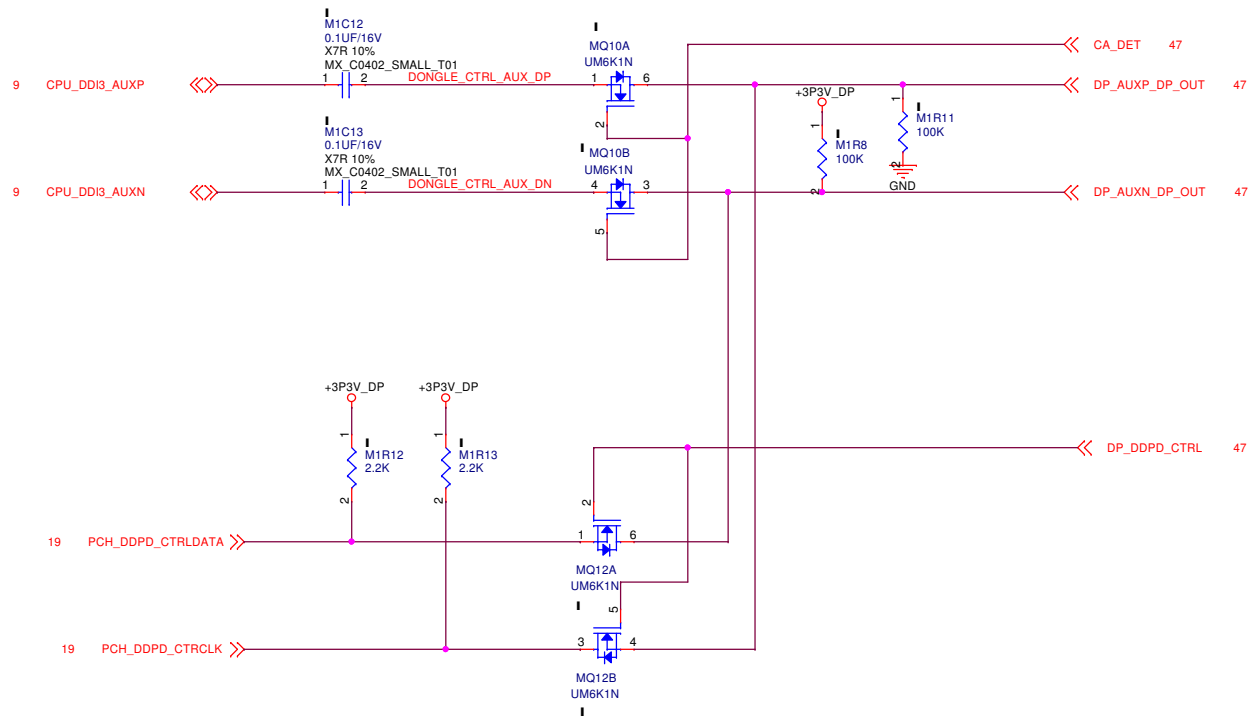








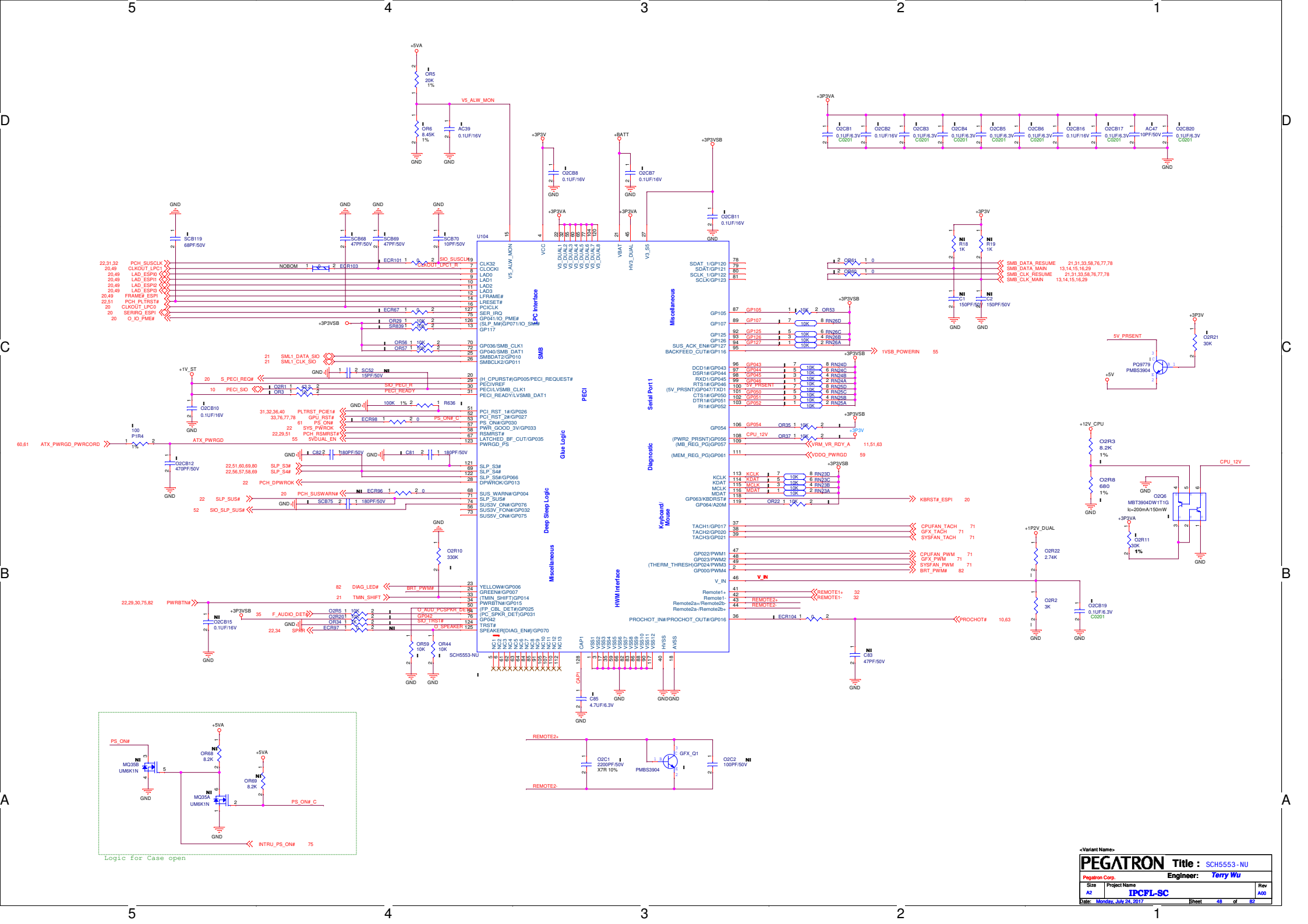


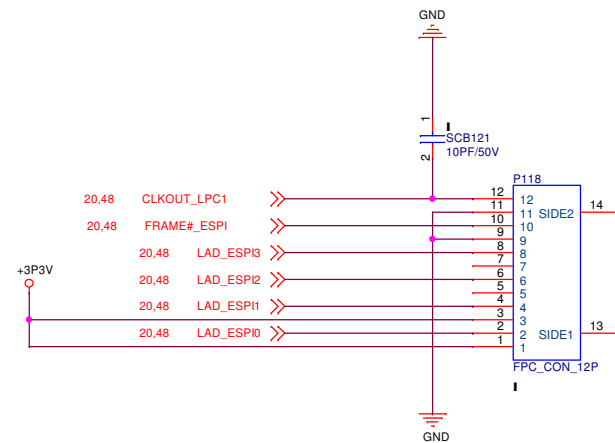


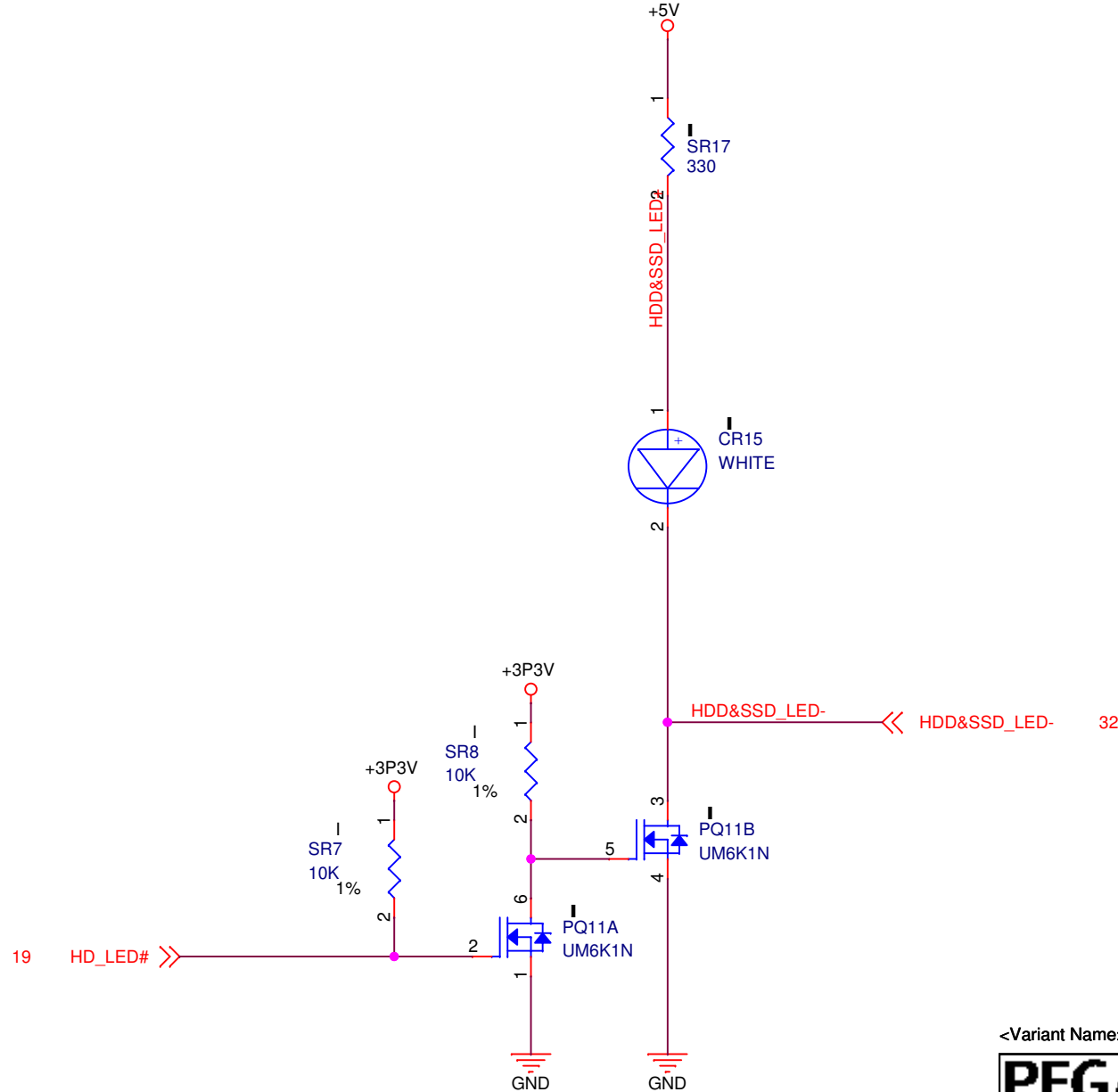
<Variant Name>

PEGATRON		Title : DP DONGLE CTRL	
Pegatron Corp.		Engineer: Terry Wu	
Size A3	Project Name IPCFL-SC	Rev A00	
Date: Monday, July 24, 2017		Sheet 46 of 82	



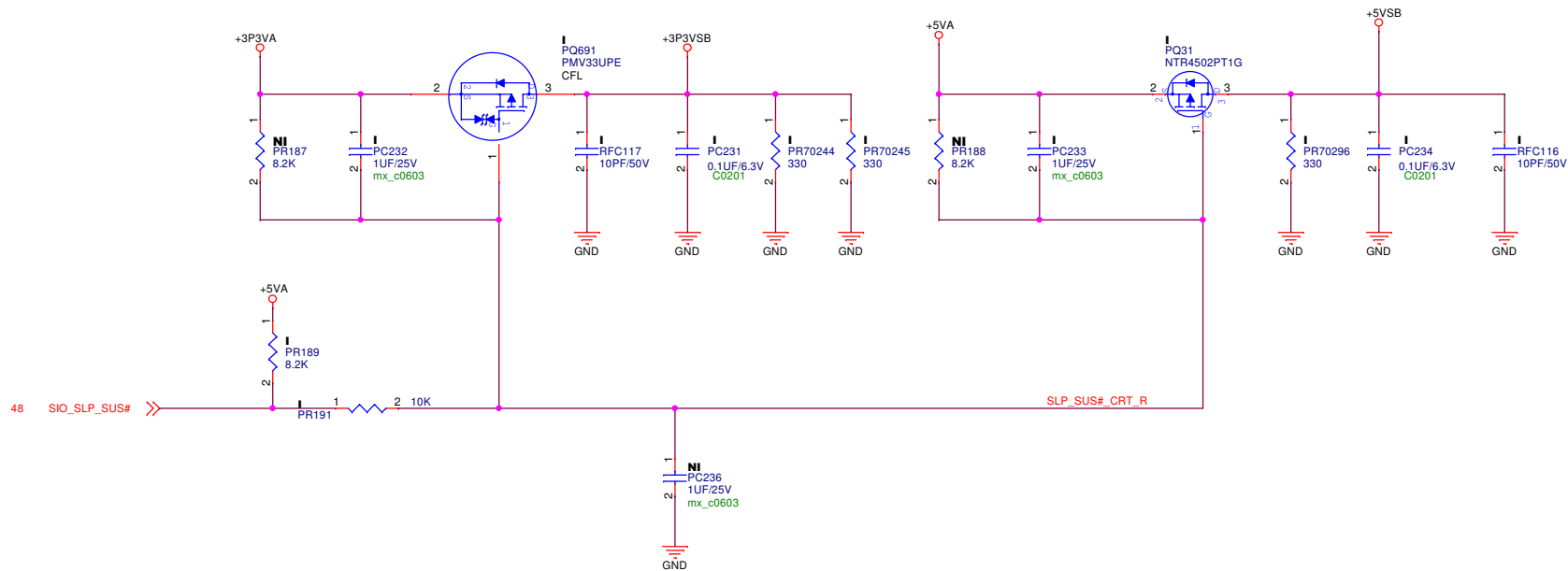






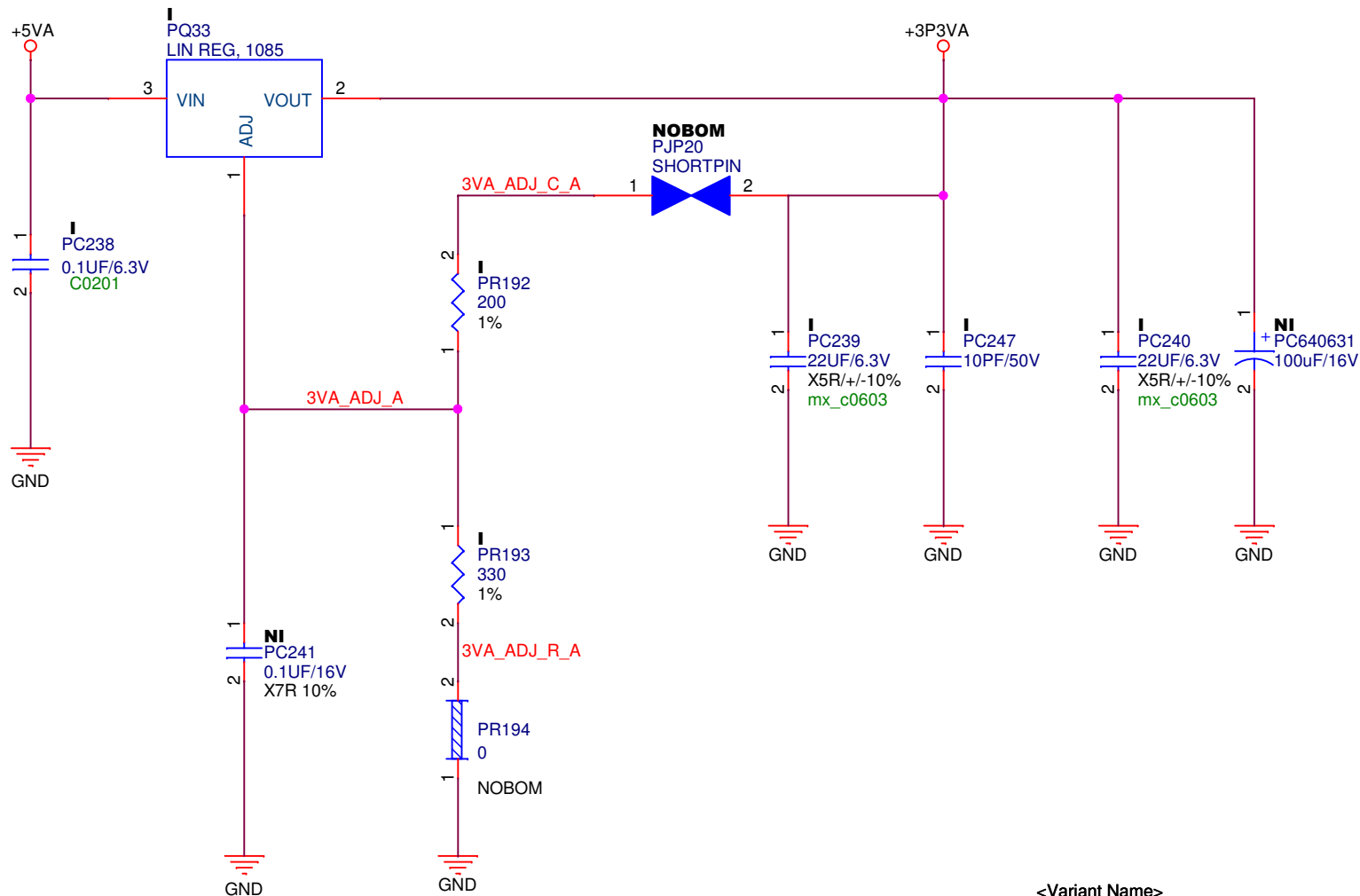
<Variant Name>

PEGATRON		Title :	
Pegatron Corp.		Engineer: Terry Wu	
Size A	Project Name IPCFL-SC		Rev A00
Date: Monday, July 24, 2017	Sheet 50 of 82		



<Variant Name>

PEGATRON		Title : +3V / 5VSB / +3VA	
Pegatron Corp.		Engineer: Terry Wu	
Size A3	Project Name IPCFL-SC		Rev A00
Date: Monday, July 24, 2017		Sheet 52 of 82	

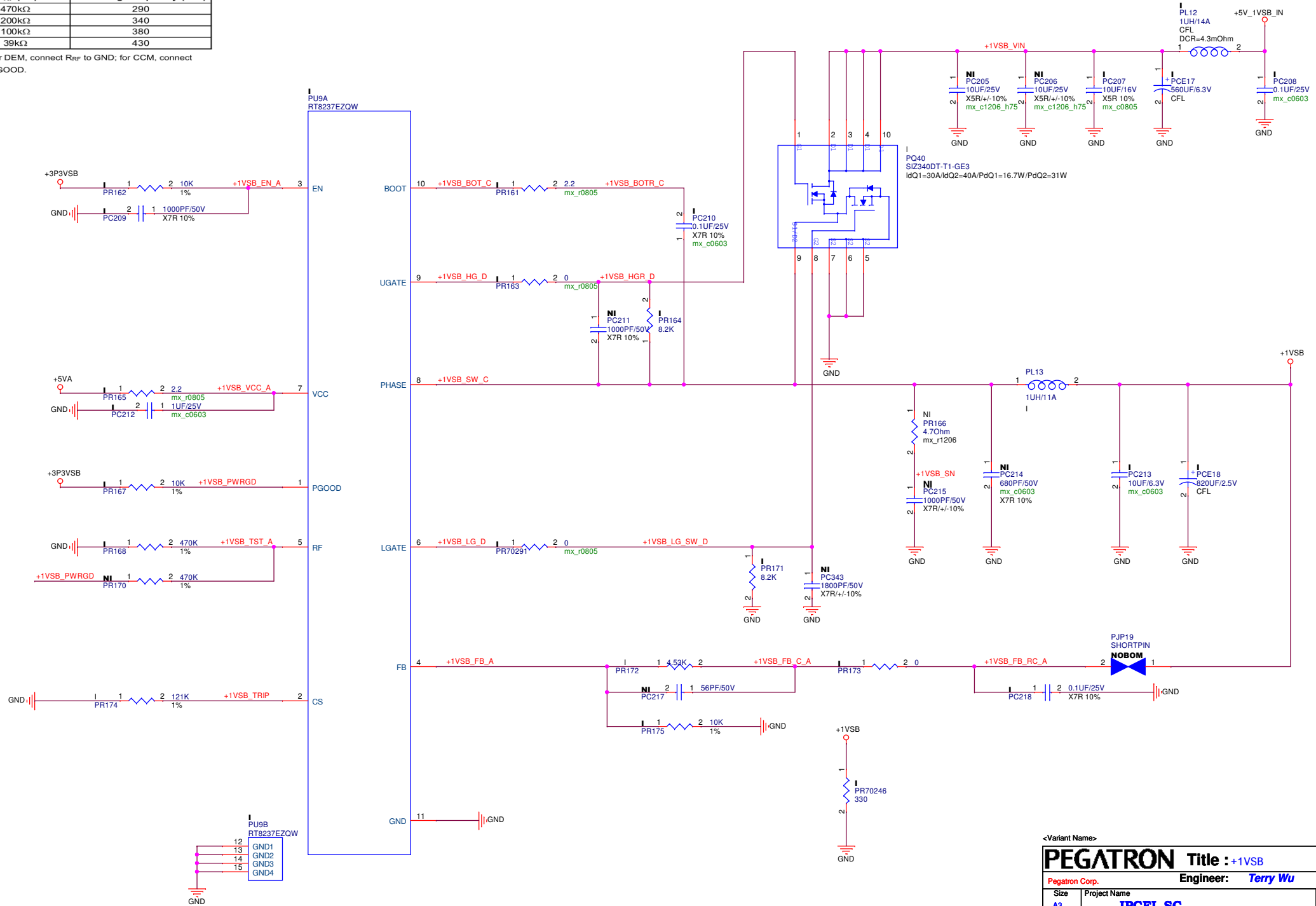


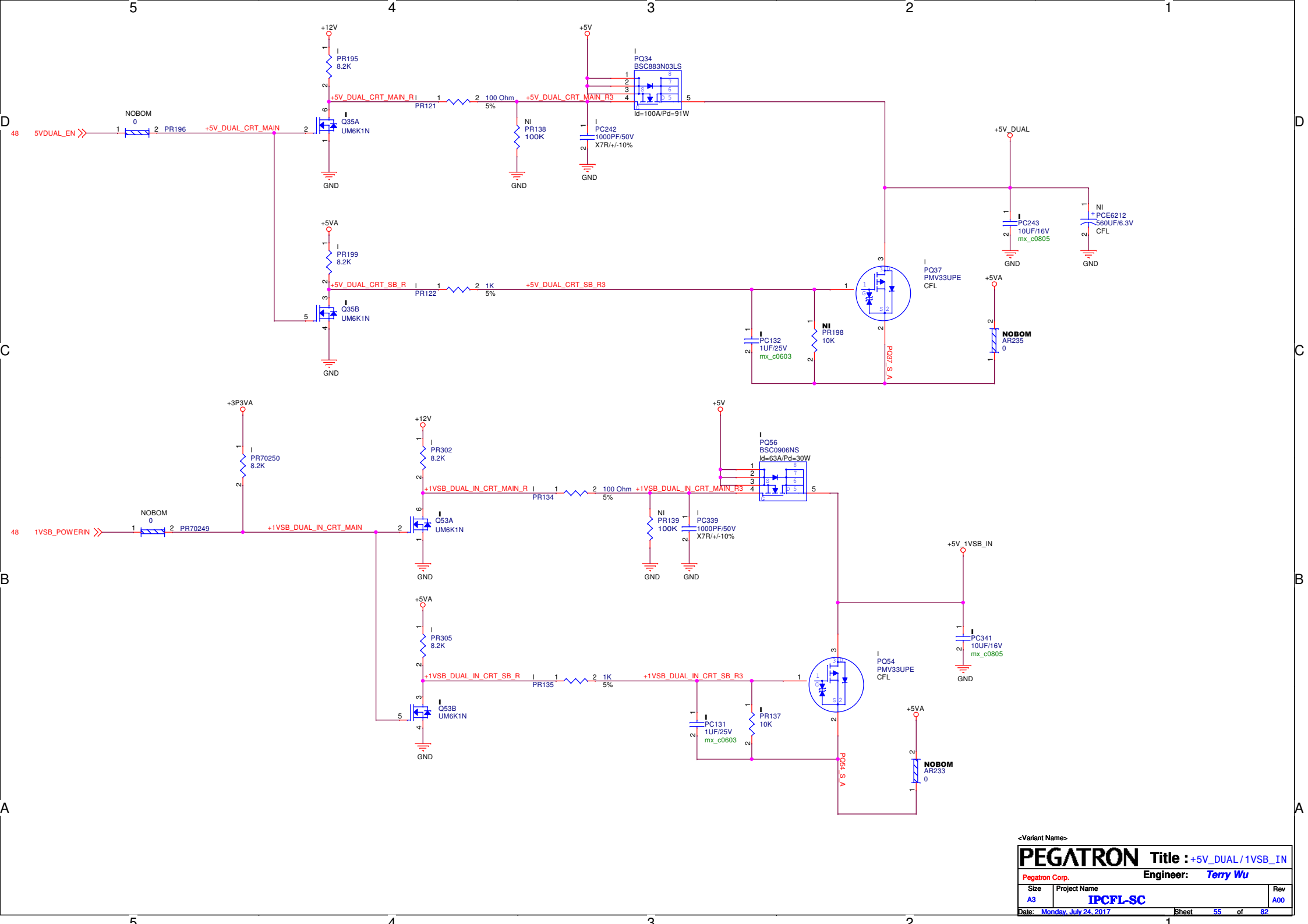
<Variant Name>

PEGATRON		Title : +3P3VA	
Pegatron Corp.		Engineer: Terry Wu	
Size A	Project Name IPCFL-SC		Rev A00
Date: Monday, July 24, 2017		Sheet 53	of 82

R _{RF} (kΩ)	Switching Frequency (kHz)
470kΩ	290
200kΩ	340
100kΩ	380
39kΩ	430

Note : For DEM, connect R_{RF} to GND; for CCM, connect R_{RF} to PGOOD.





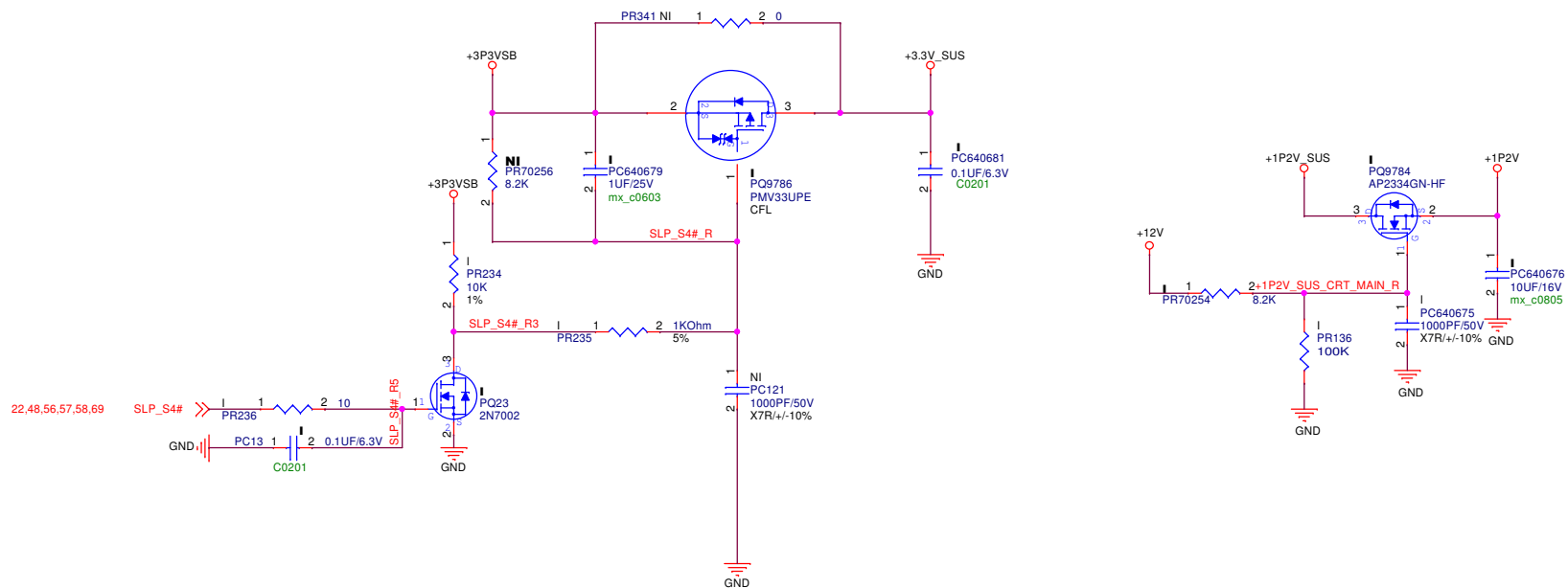
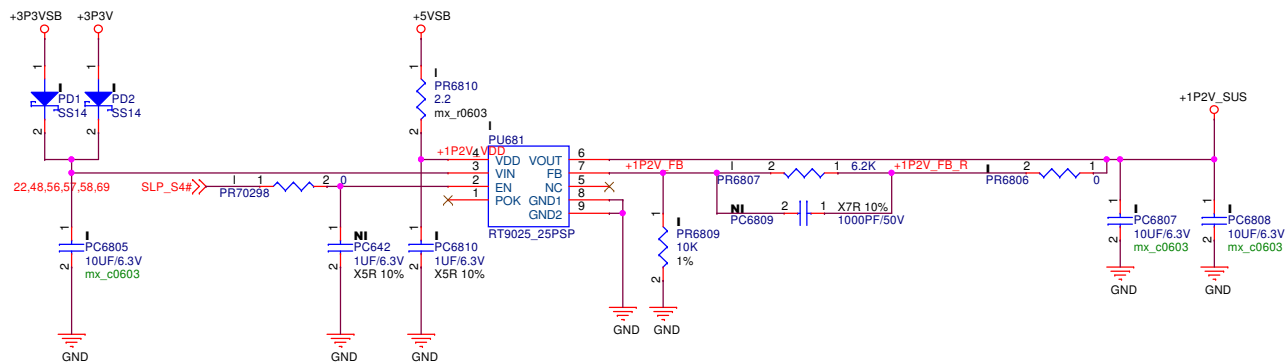
5

4

3

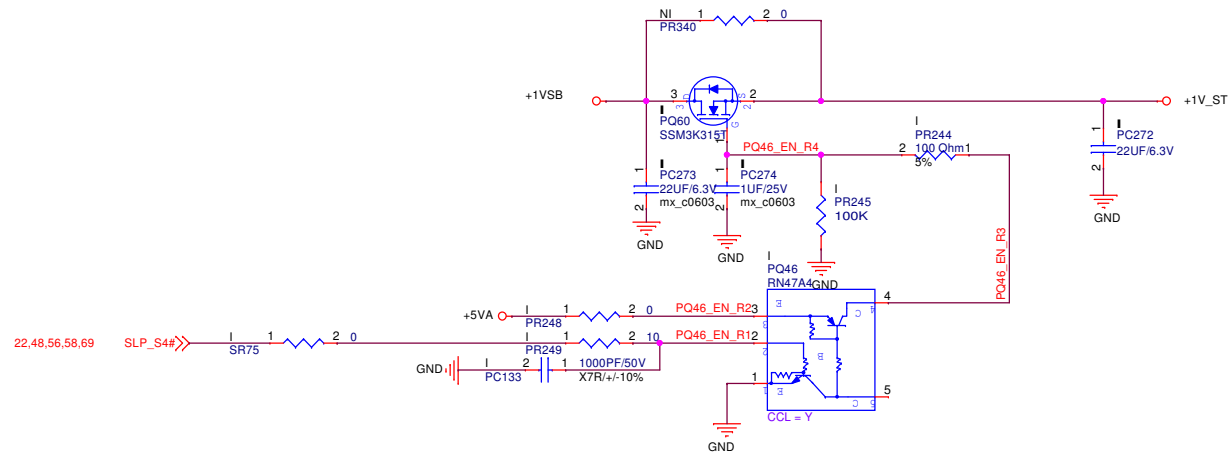
2

1



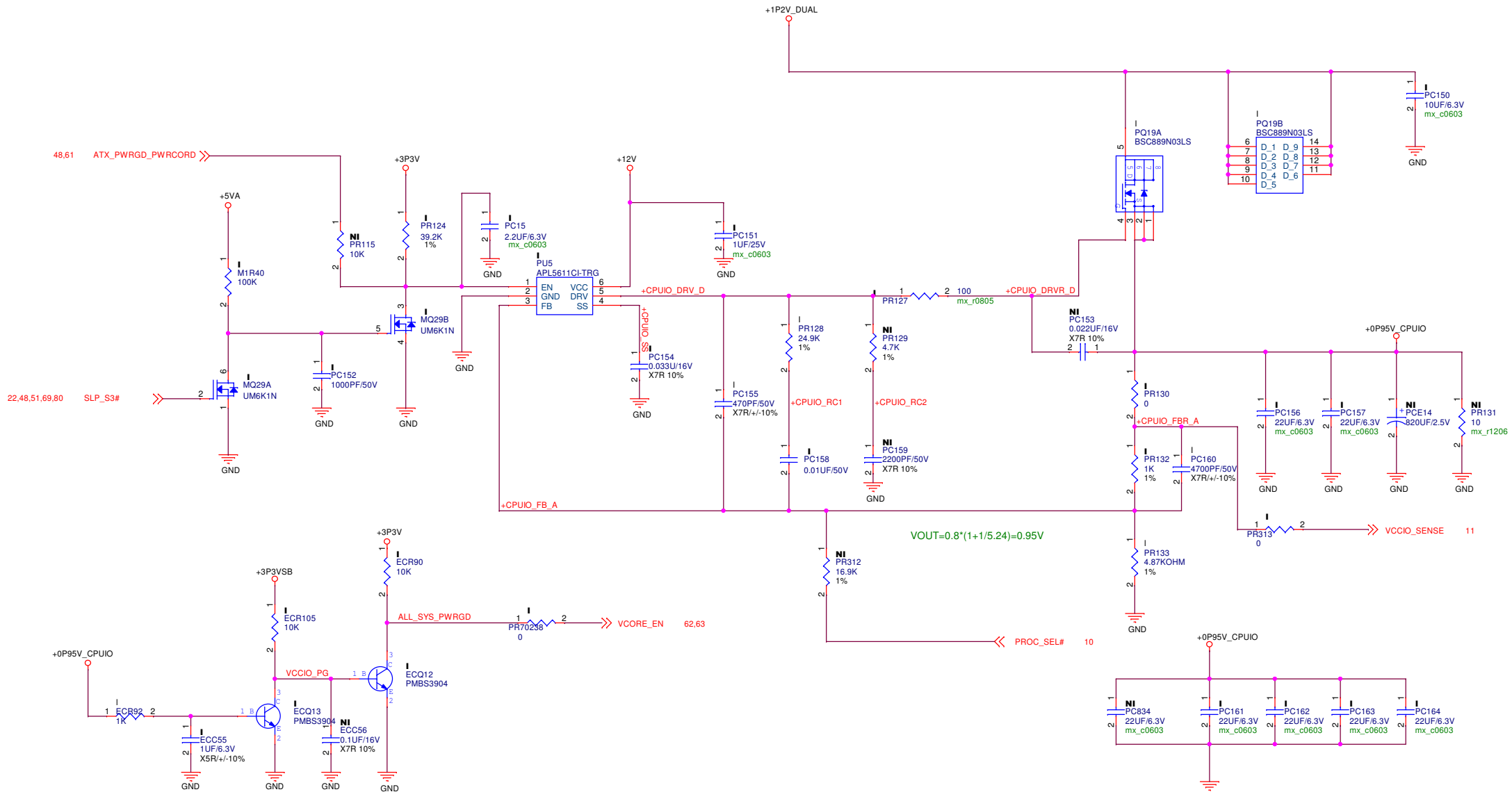
<Variant Name>

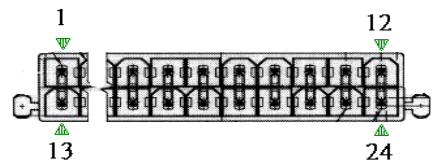
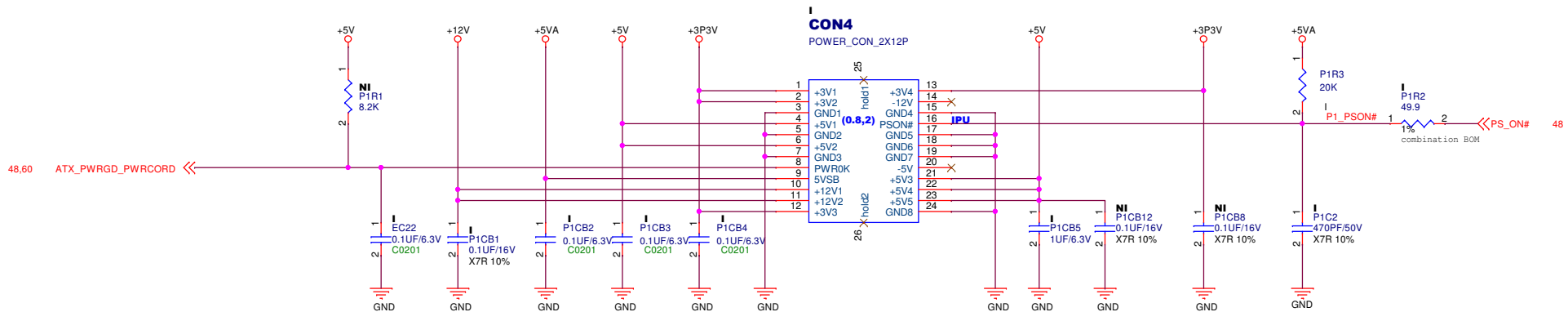
PEGATRON		Title : +1P2V	
Pegatron Corp.		Engineer: Terry Wu	
Size	Project Name		Rev
A3	IPCFL-SC		A00
Date: Monday, July 24, 2017		Sheet	56 of 82



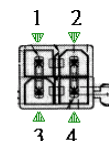
<Variant Name>

PEGATRON		Title : +1P2V	
Pegatron Corp.		Engineer: <i>Terry Wu</i>	
Size A3	Project Name IPCFL-SC		Rev A00
Date: Monday, July 24, 2017	Sheet	57	of 82

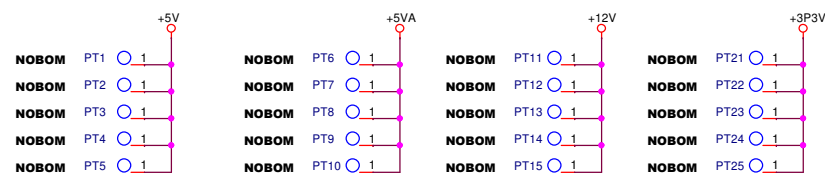
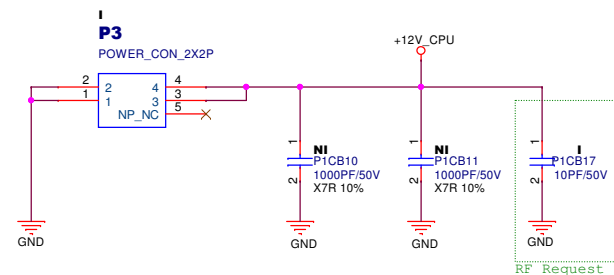




TOP SIDE VIEW

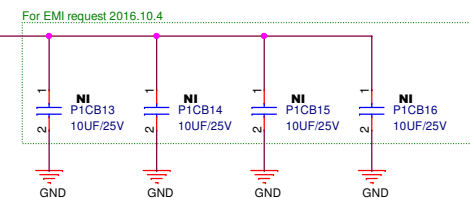
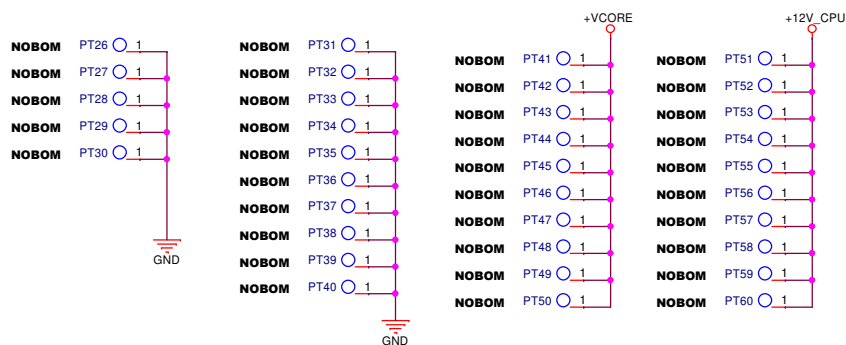


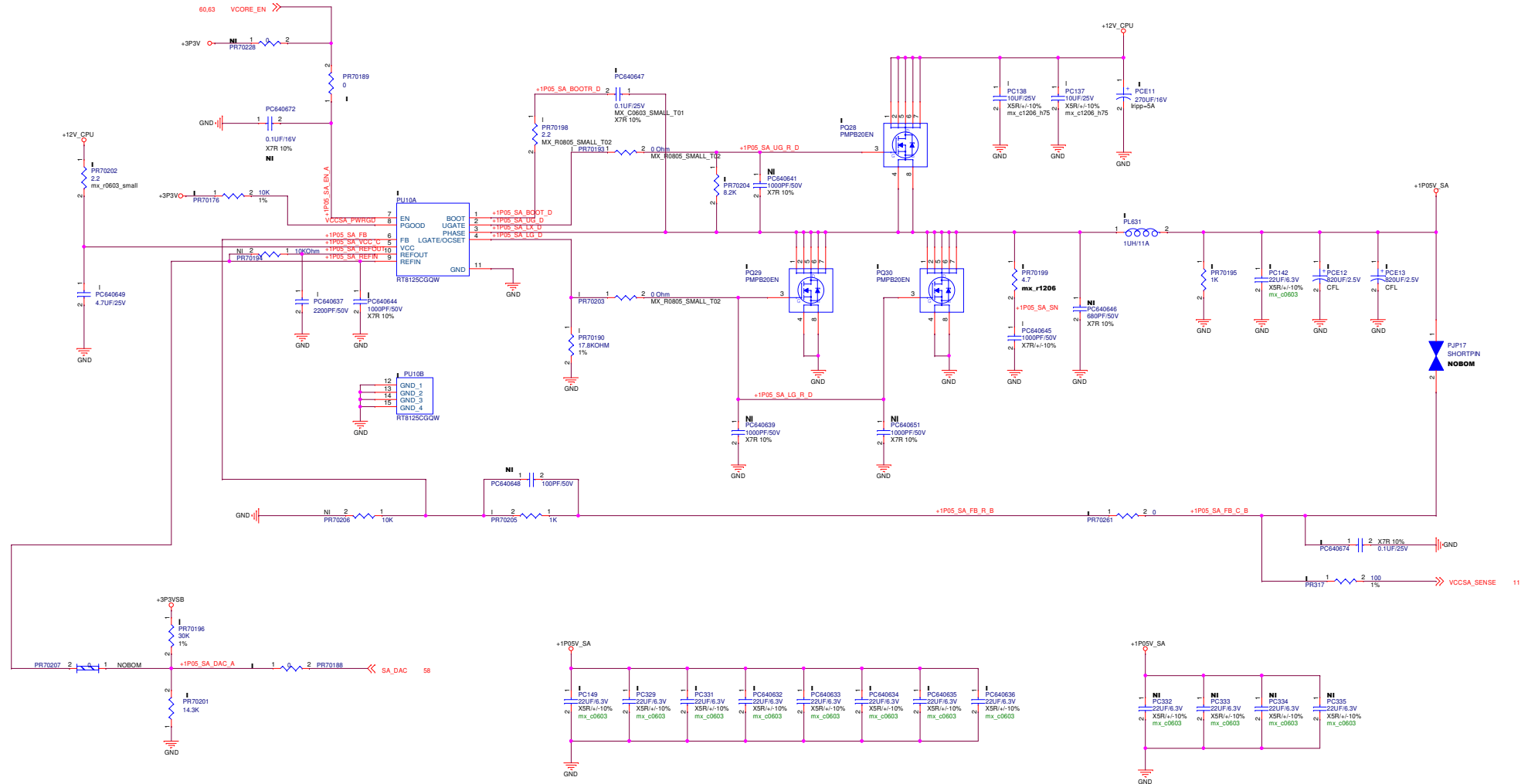
TOP SIDE VIEW

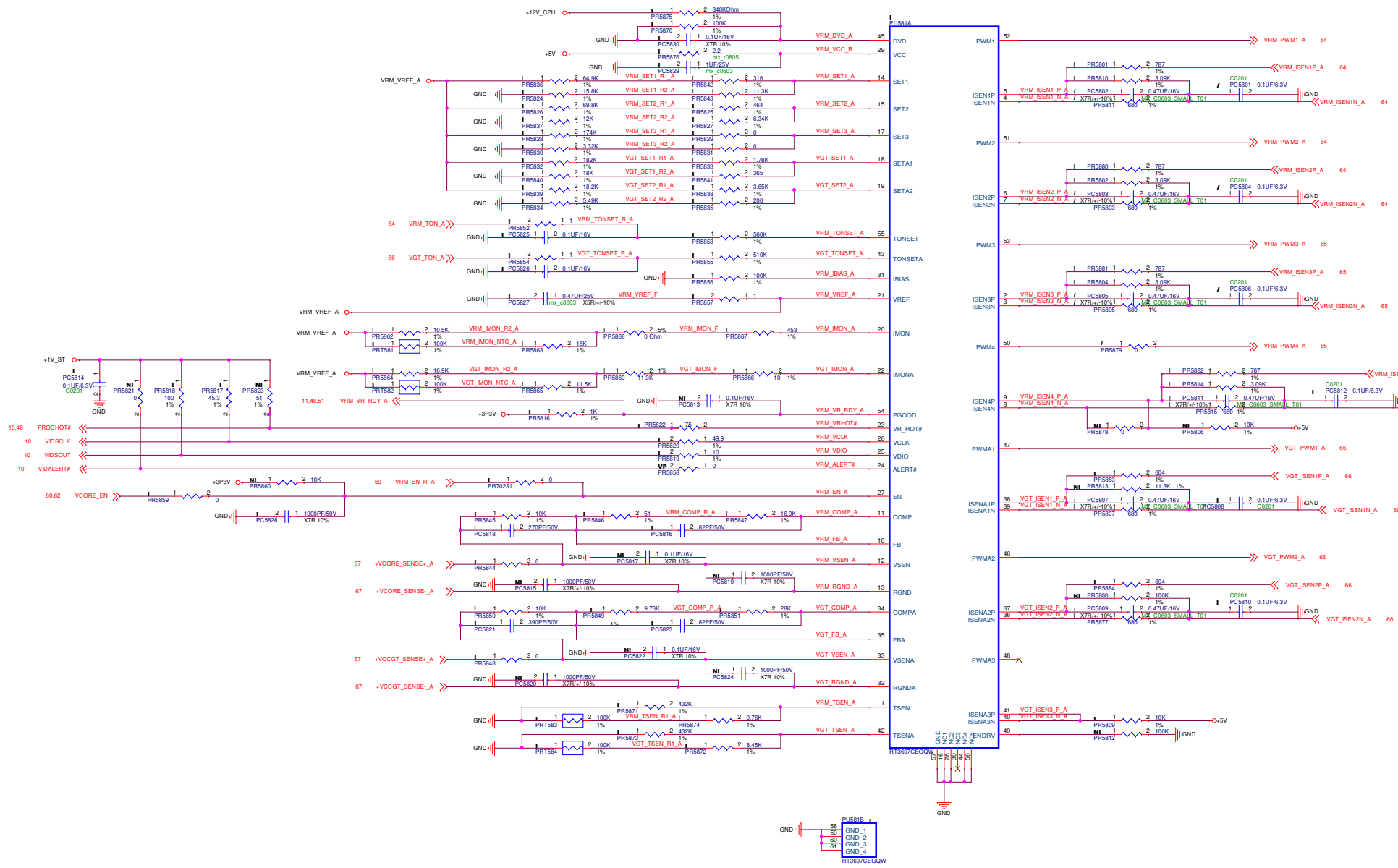


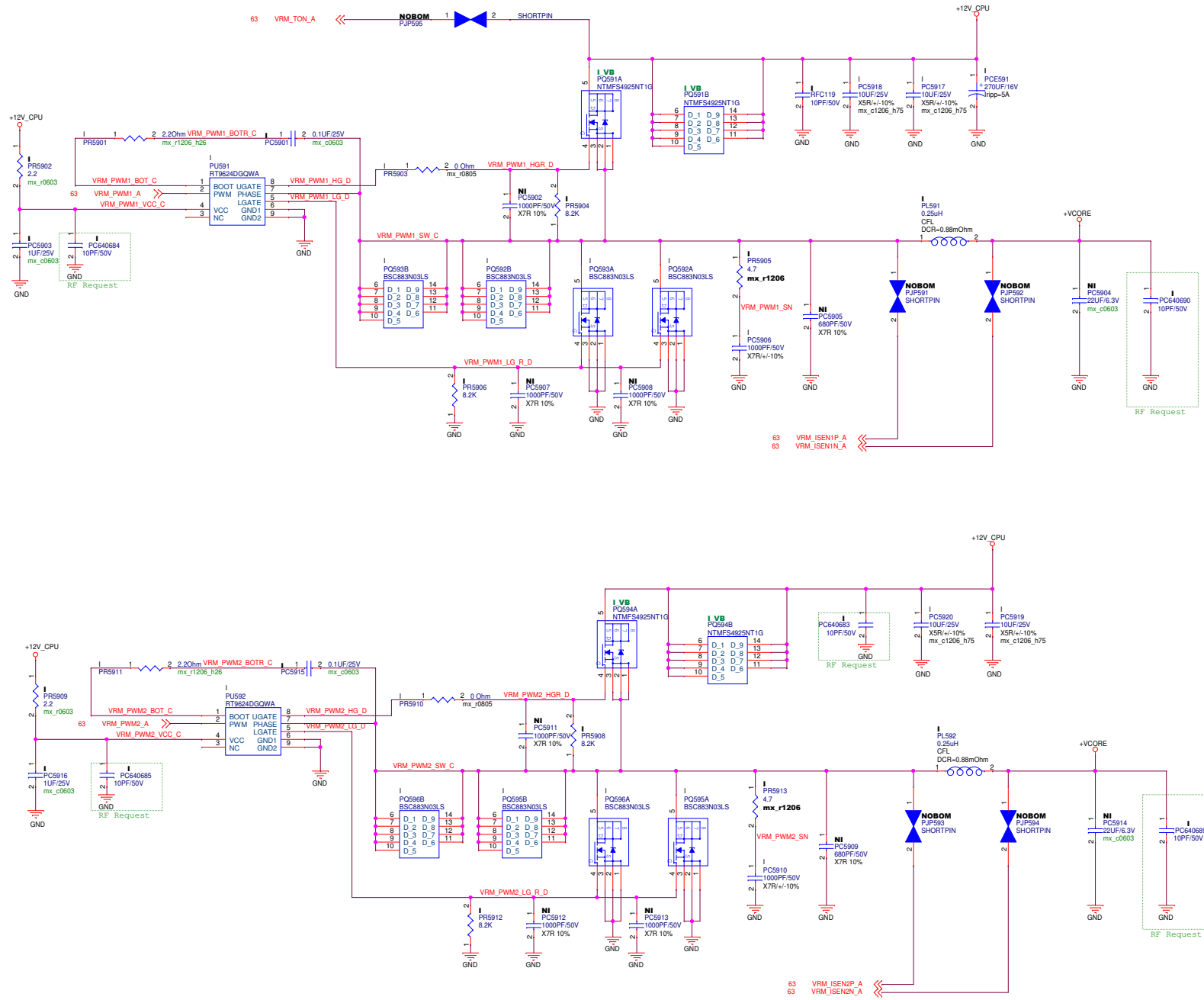
Nodes related to different power planes

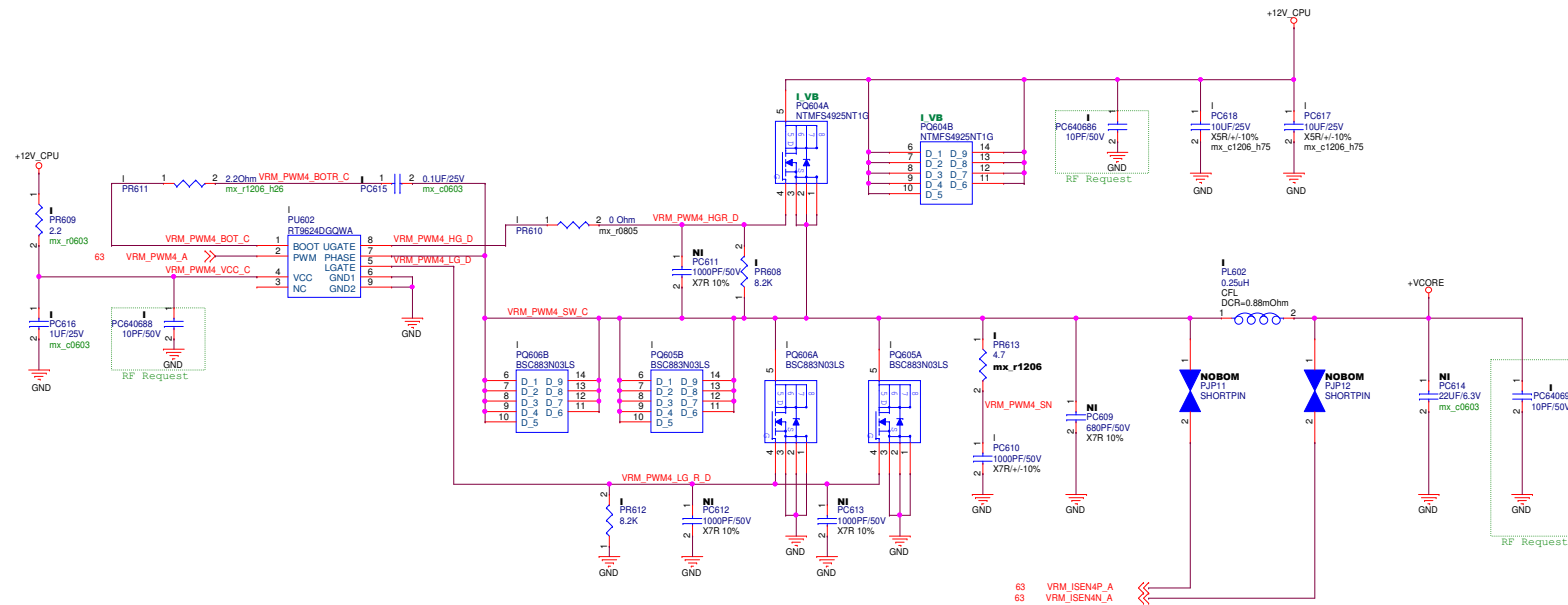
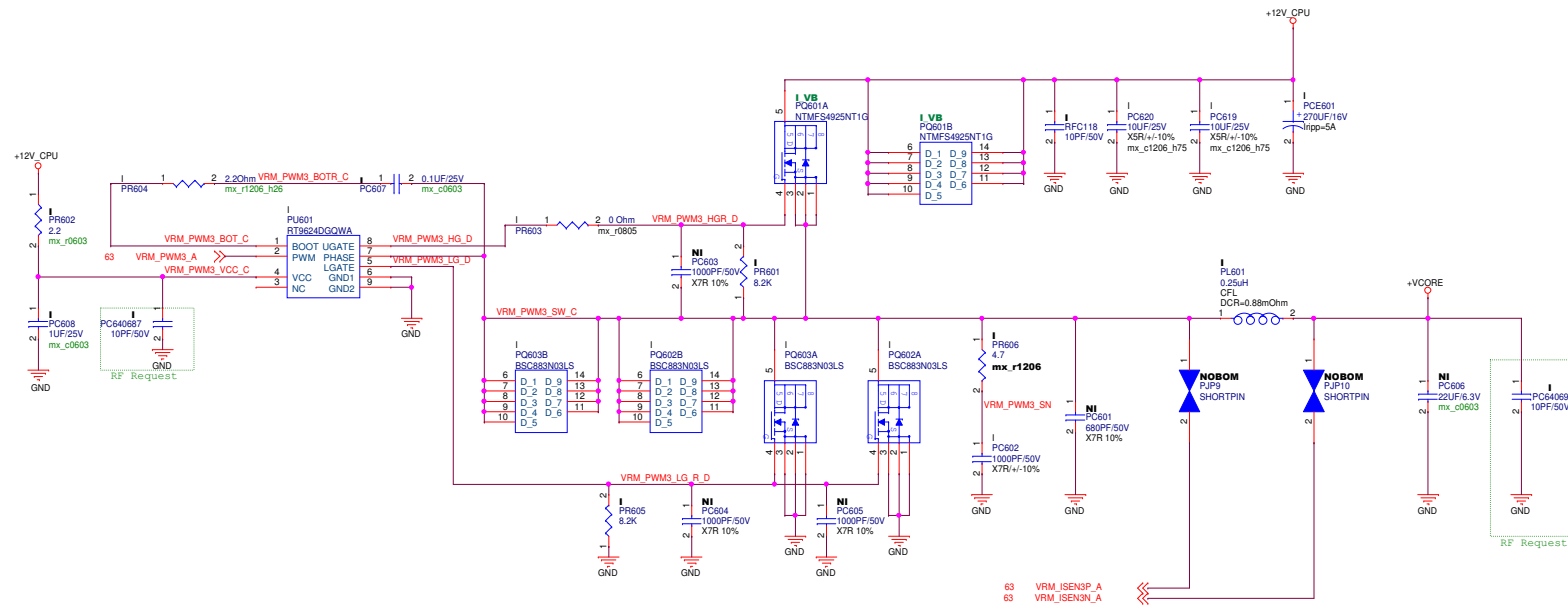
Node	Goal Q'ty
+5V	5
+5VA	5
+12V	5
-12V	5
+3V	5
+Vcore	10
+GND	15
+12V_CPU	10

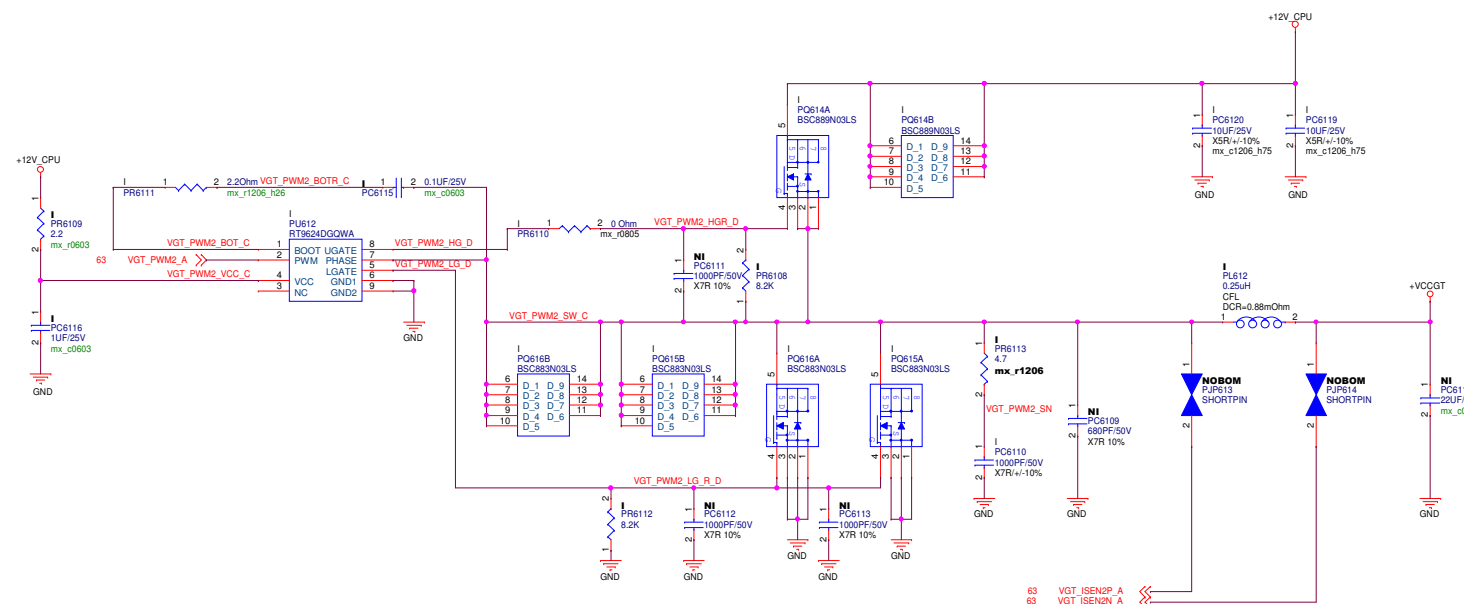
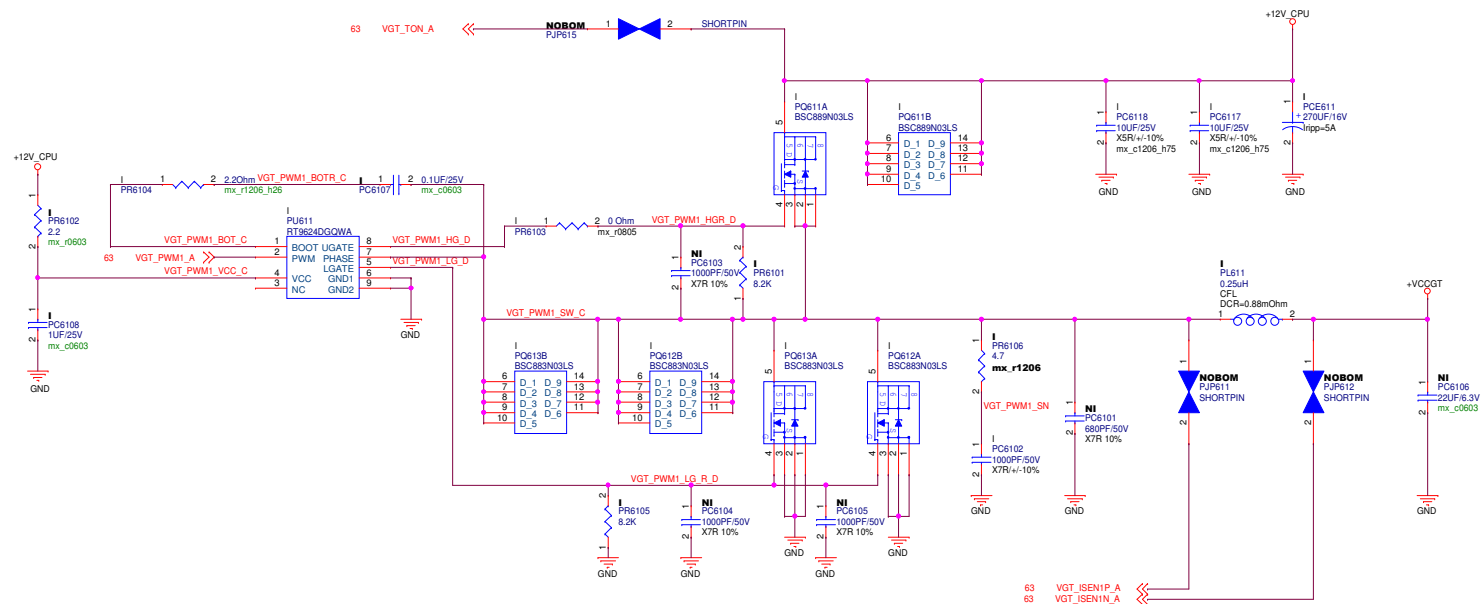


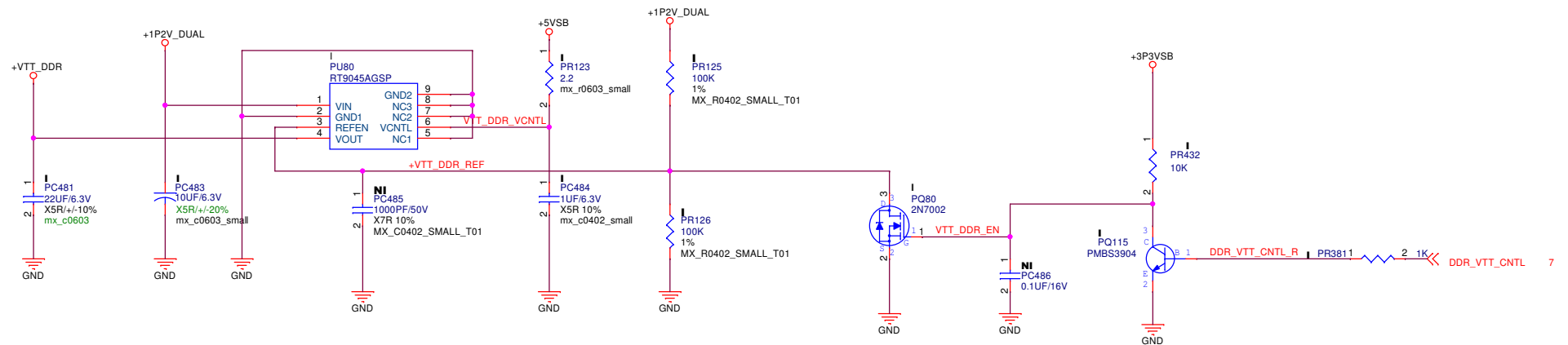


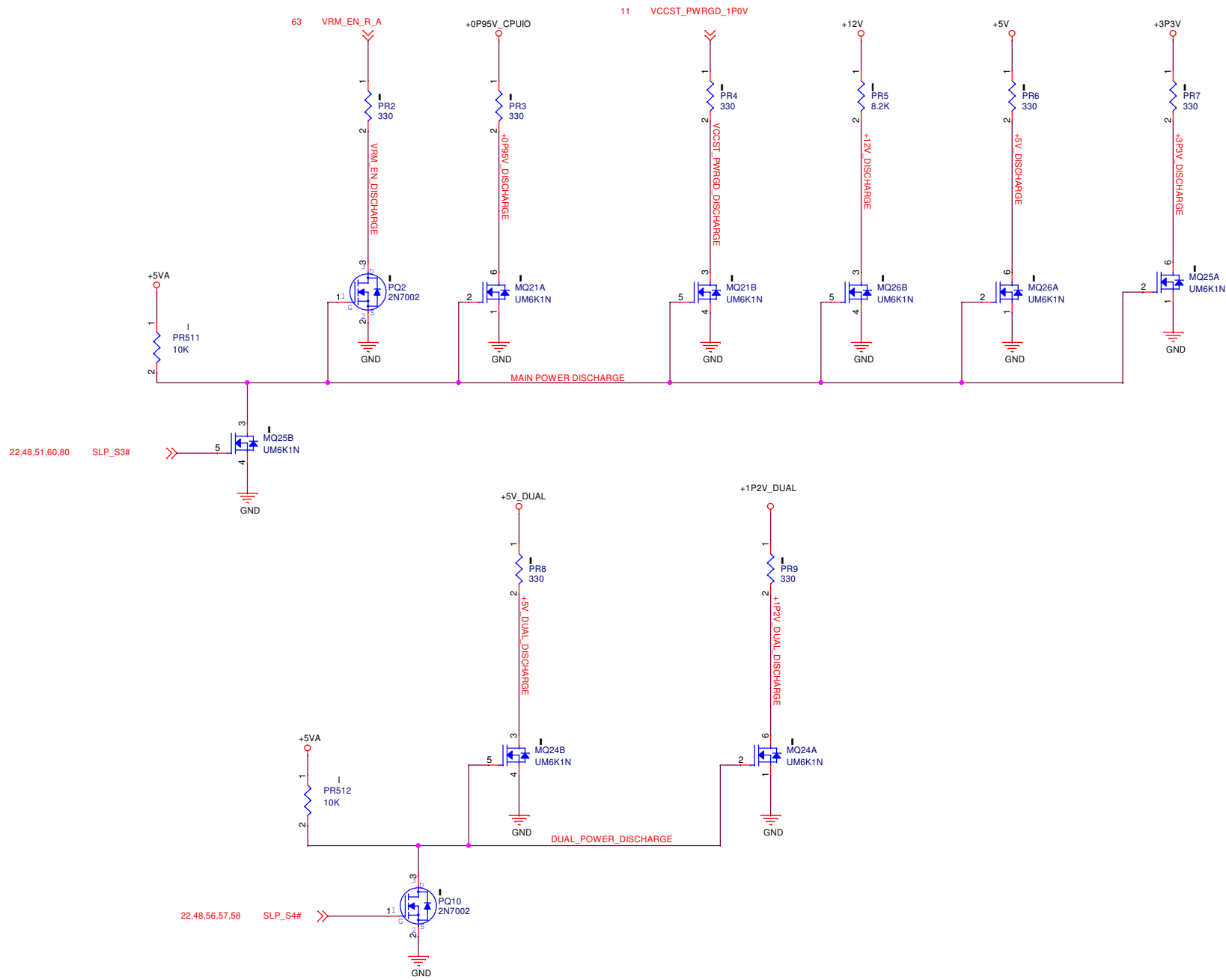








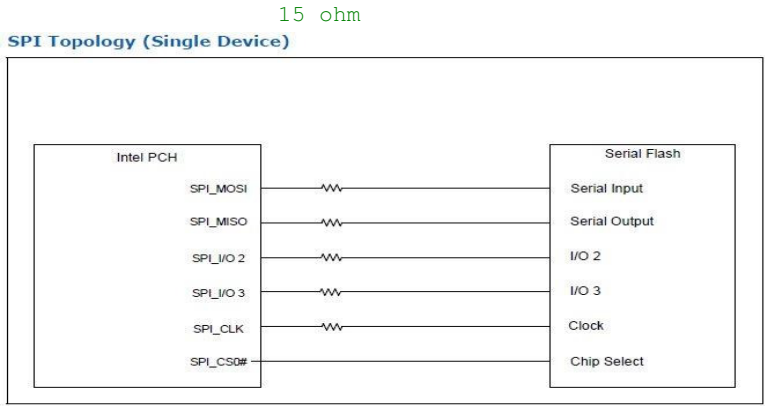
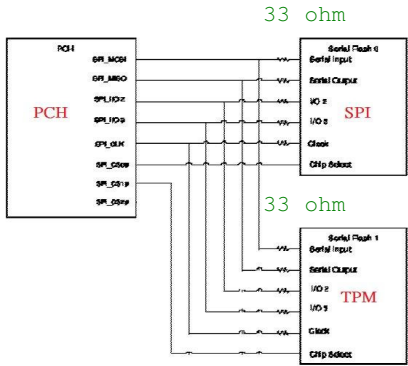




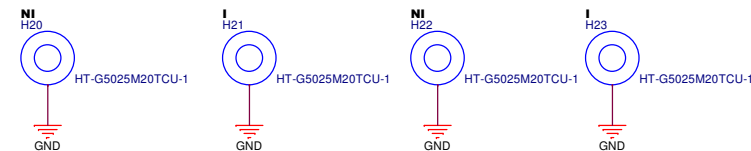
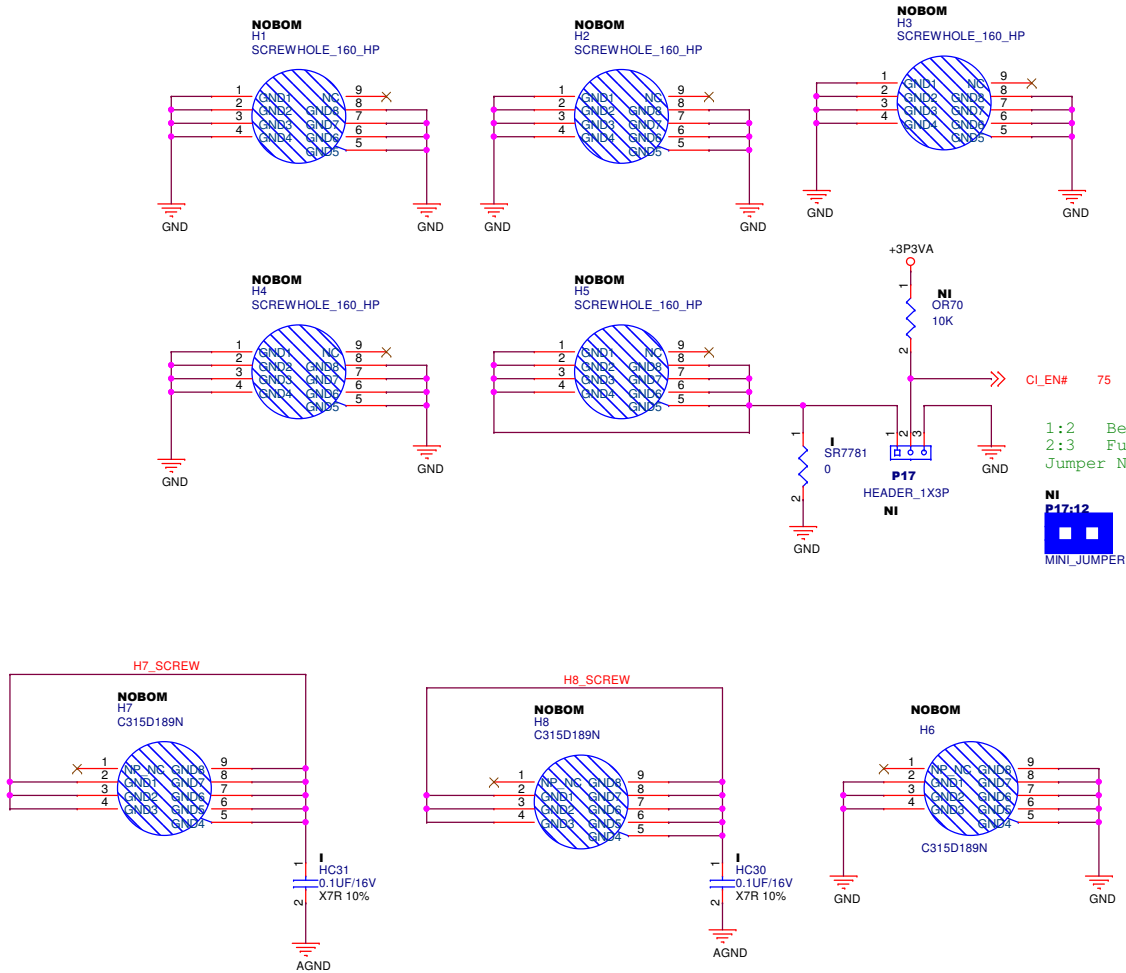


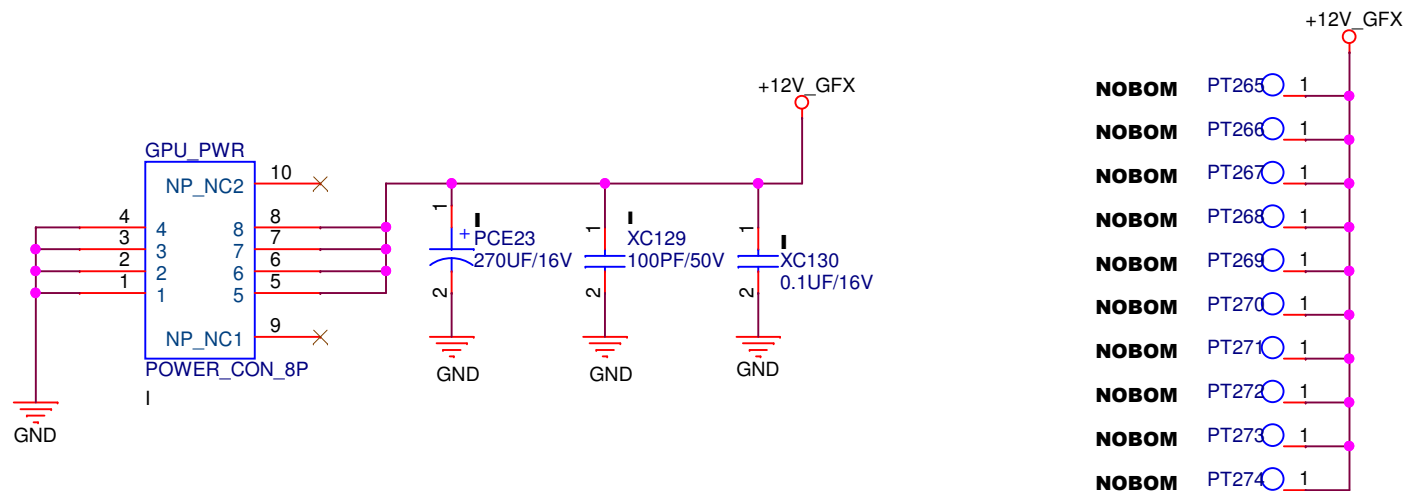
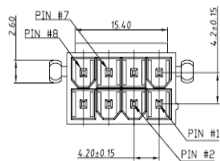
<Variant Name>

PEGATRON		Title : NUT	
Pegatron Corp.		Engineer: Terry Wu	
Size	Project Name		Rev
A3	IPCFL-SC		A00
Date: Monday, July 24, 2017		Sheet 70 of 82	1



<Variant Name>			
PEGATRON		Title : TPM	
Pegatron Corp.		Engineer: Terry Wu	
Size	Project Name		Rev
B	IPCFL-SC		A00
Date: Monday, July 24, 2017		Sheet	72 of 82

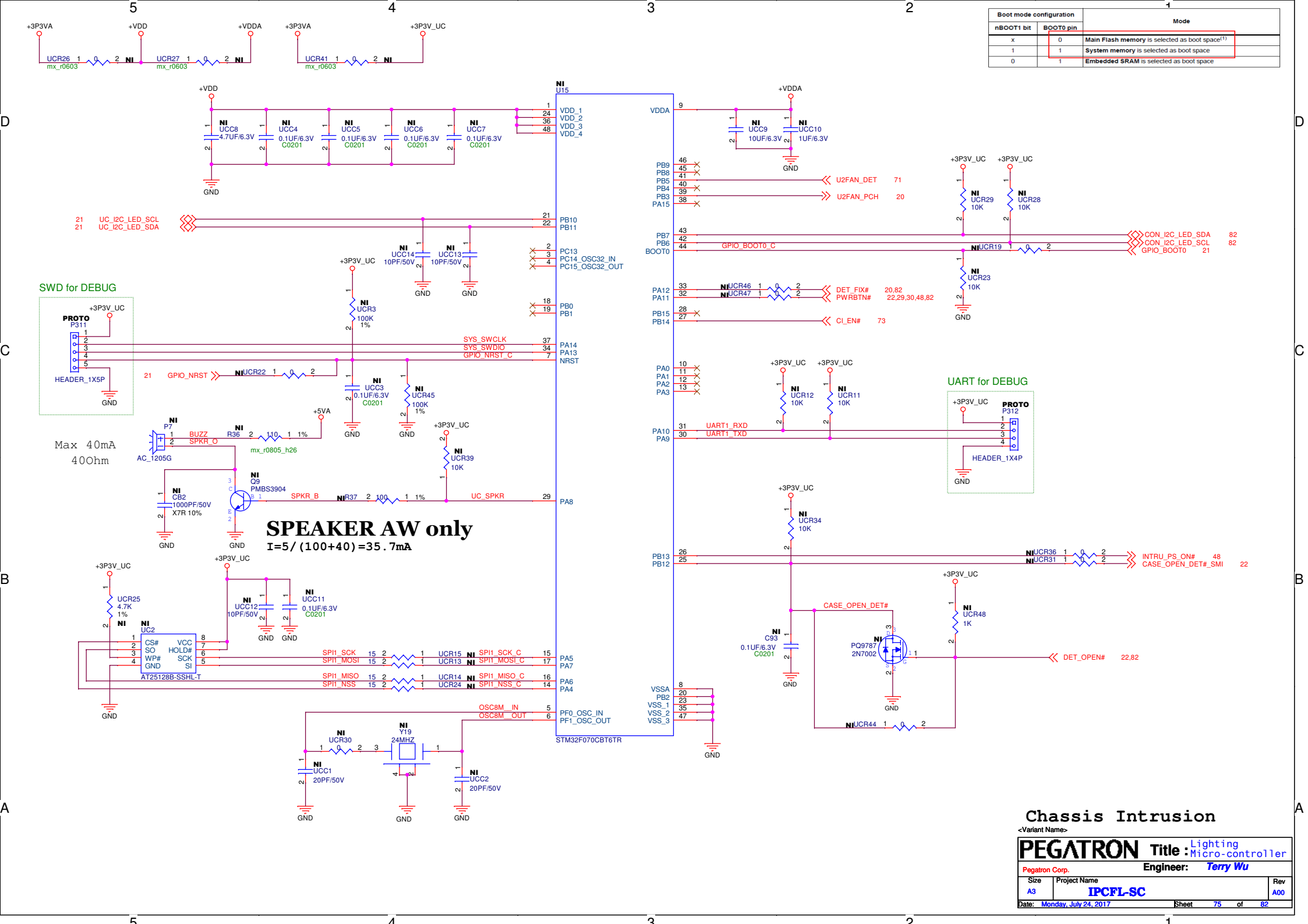


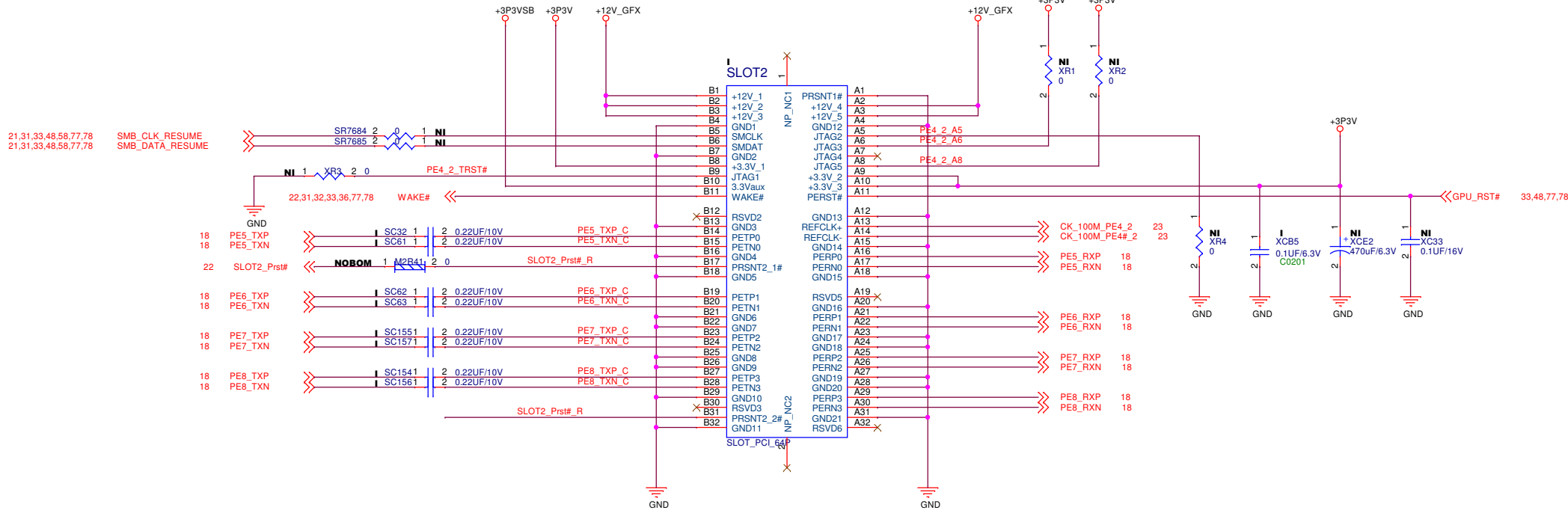


NOBOM	PT265	1
NOBOM	PT266	1
NOBOM	PT267	1
NOBOM	PT268	1
NOBOM	PT269	1
NOBOM	PT270	1
NOBOM	PT271	1
NOBOM	PT272	1
NOBOM	PT273	1
NOBOM	PT274	1

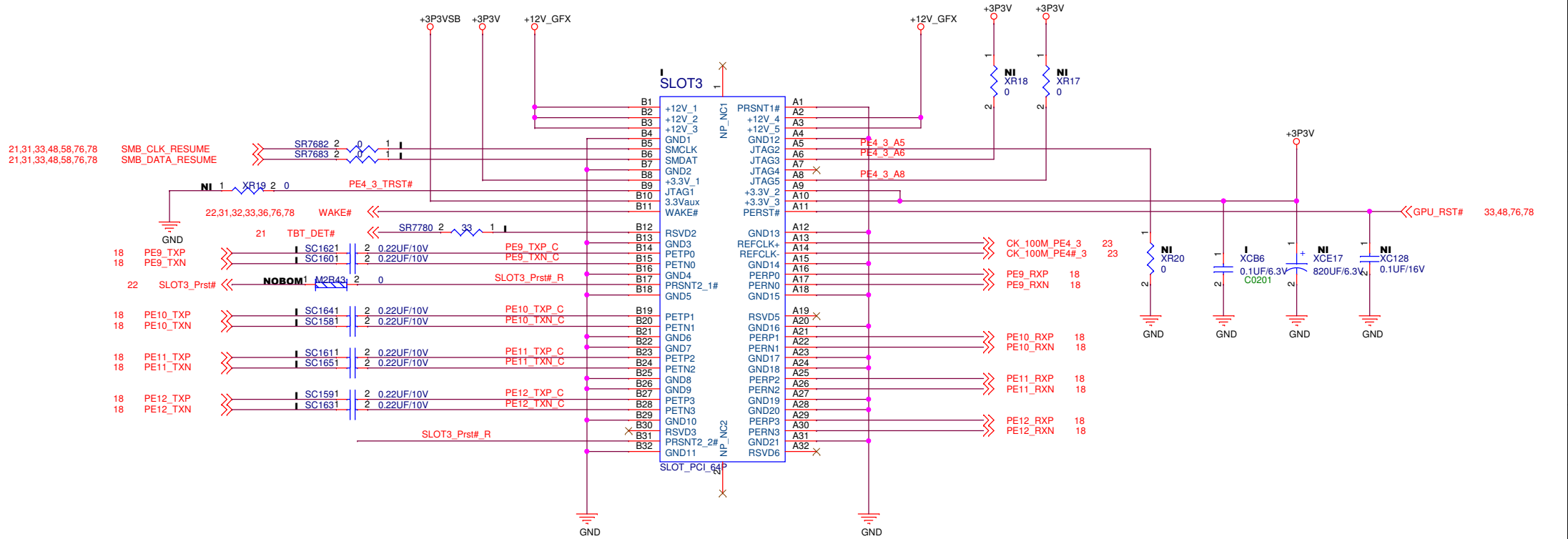
<Variant Name>

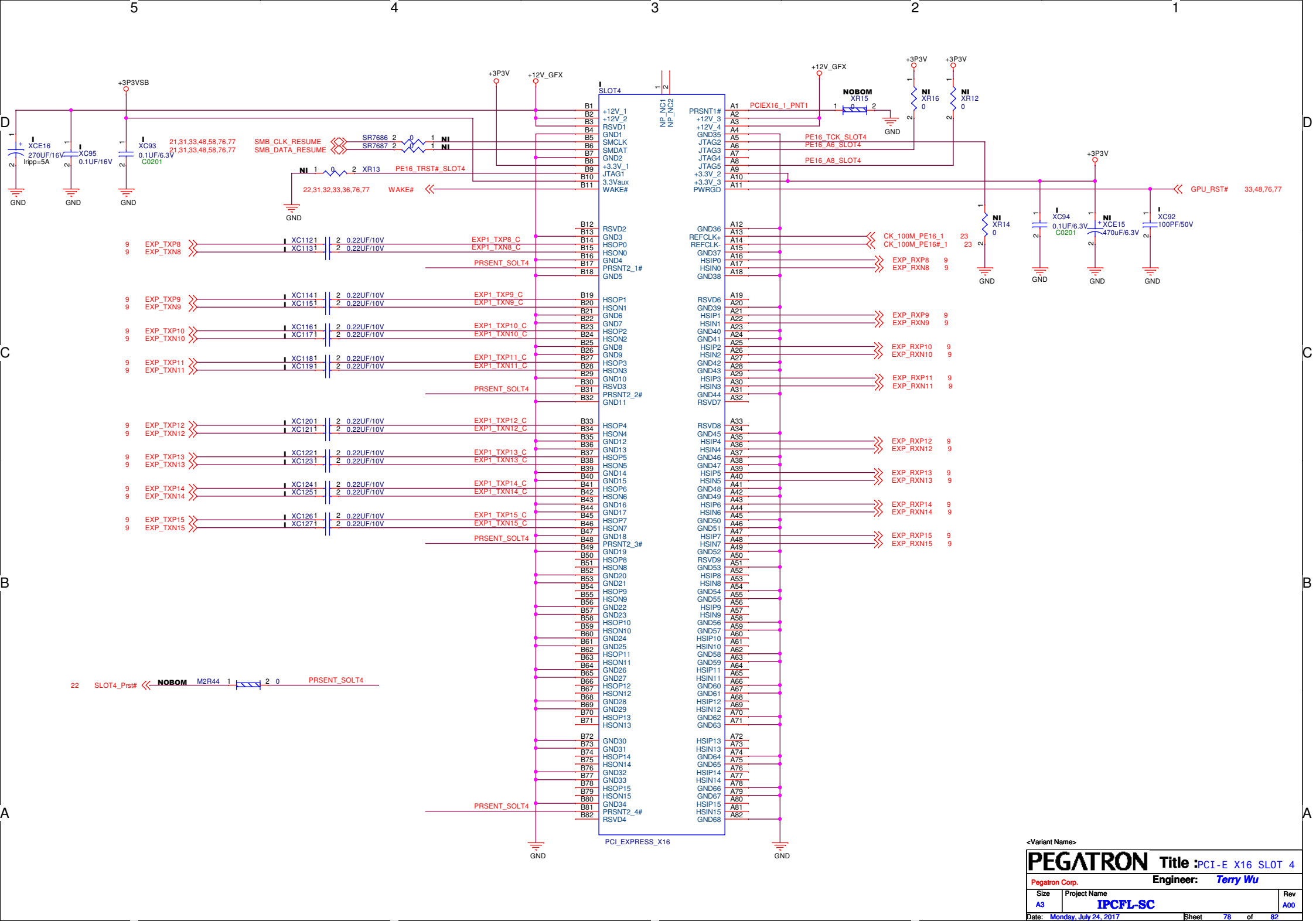
PEGATRON		Title : GPU_PWR	
Pegatron Corp.		Engineer: Terry Wu	
Size A	Project Name IPCFL-SC		Rev A00
Date: Monday, July 24, 2017	Sheet 74 of 82		



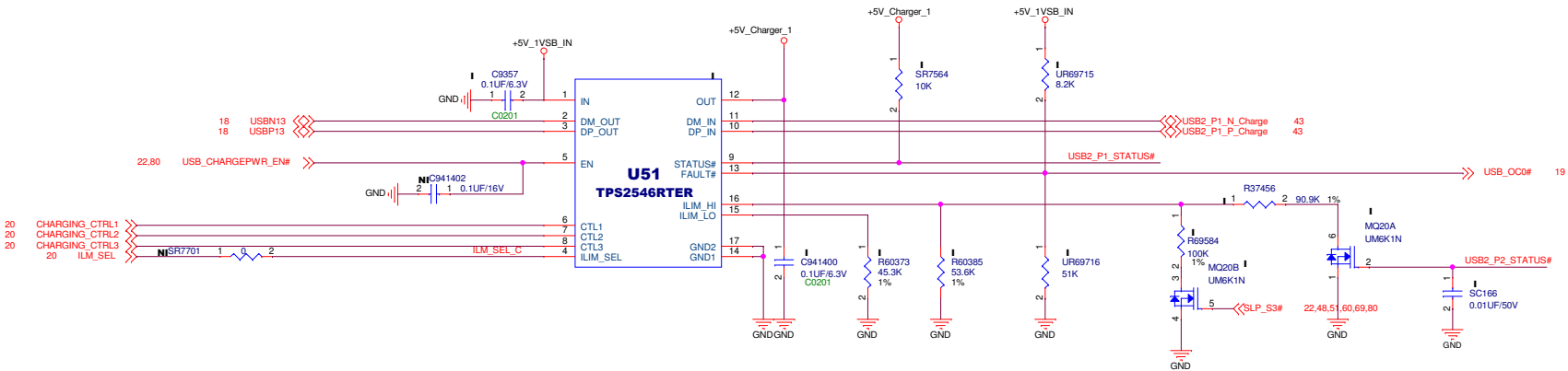


<Variant Name>

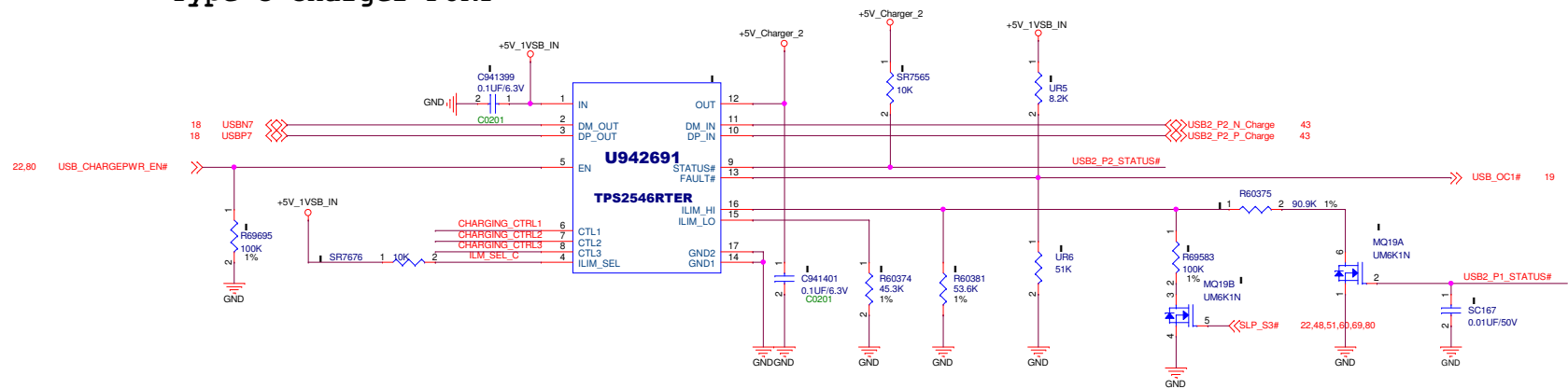




Type-A Charger PORT



Type-C Charger PORT

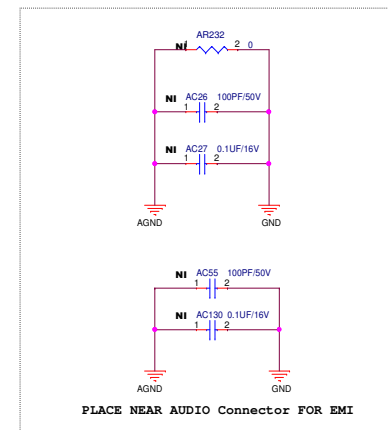
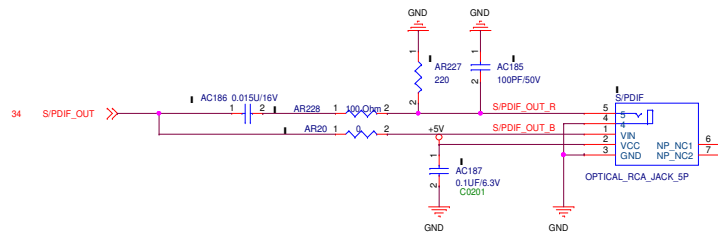
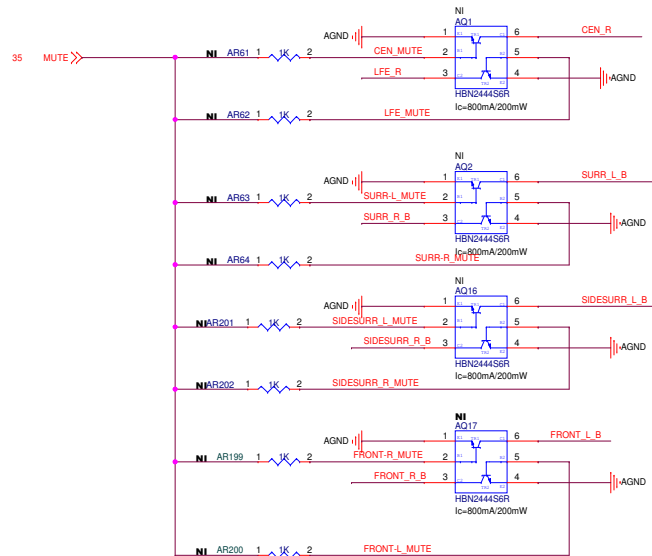
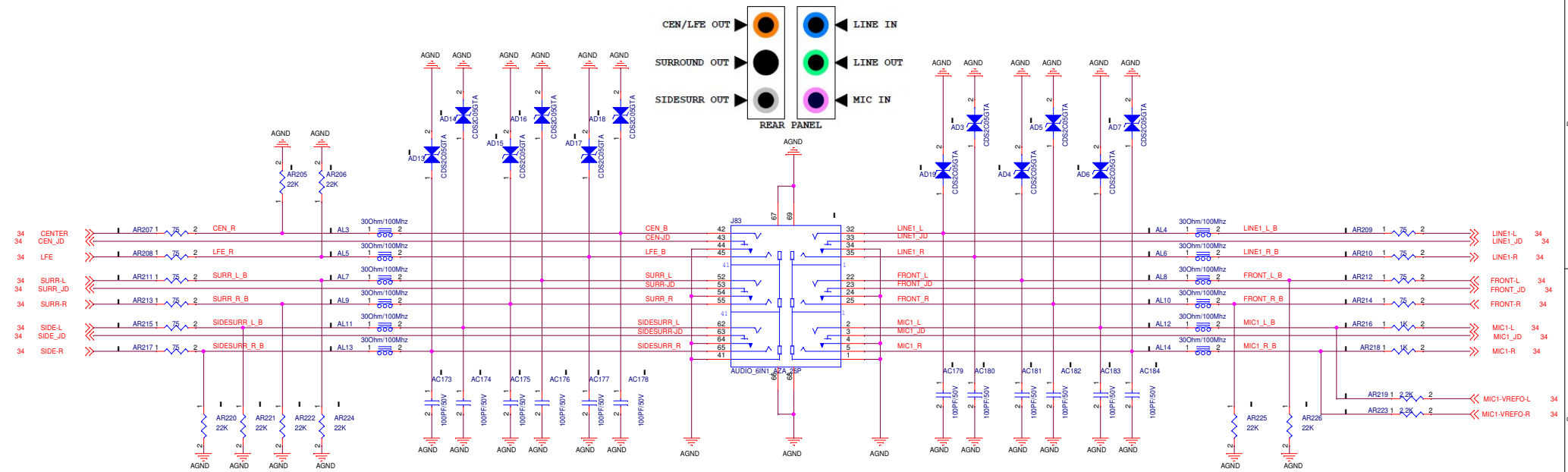


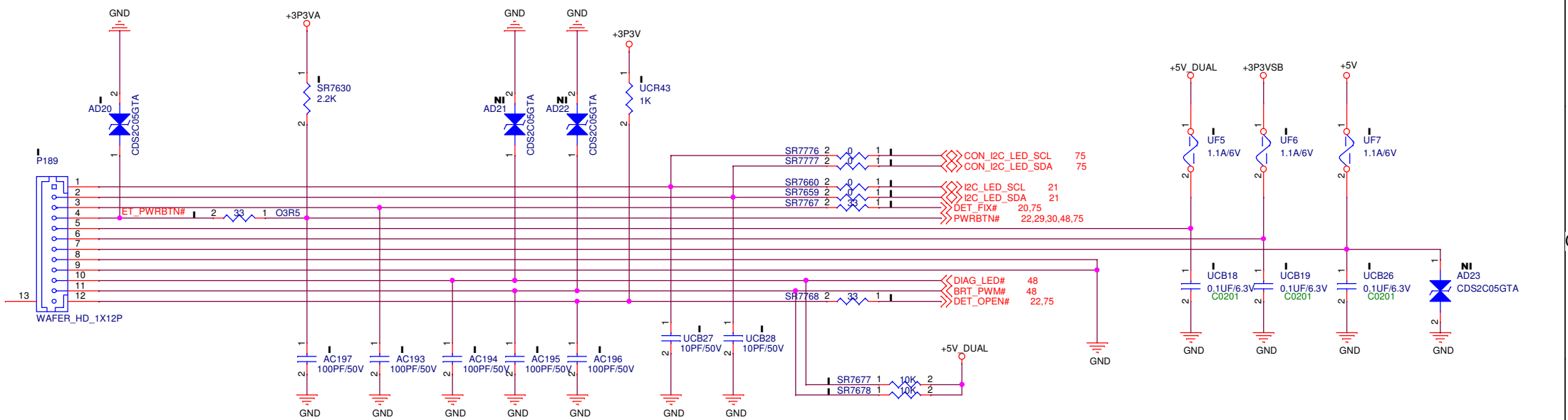
S0=53.6k//100k//90k=2A (single port charge)
S0=53.6k//100k=1.5A (dual port charge)
S345=53.6k//90k=1.5A (single port charge)
S345=53.6k=0.9A (dual port charge)

<Variant Name>

PEGATRON Title : USB CHARGING

Pegatron Corp.		Engineer: Terry Wu	
Size Custom	Project Name IPCFL-SC	Rev A00	
Date: Monday, July 24, 2017		Sheet	80 of 82





<Variant Name>

PEGATRON		Title : LED DRIVER	
Pegatron Corp.		Engineer: Terry Wu	
Size B	Project Name IPCFL-SC		Rev A00
Date: Monday, July 24, 2017		Sheet 82 of 82	